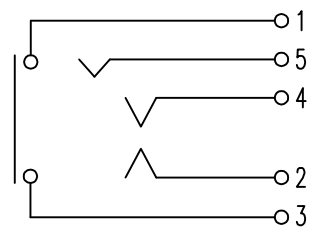
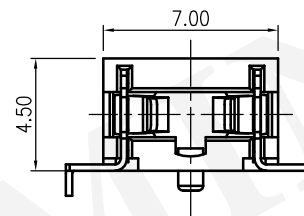
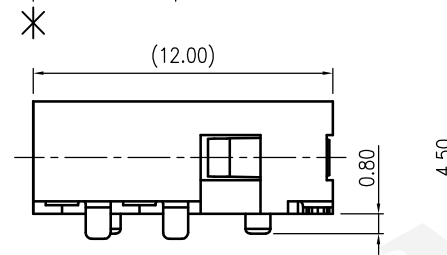
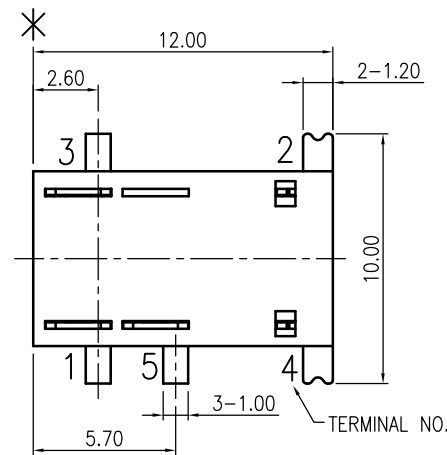


REVISIONS

LTR	DESCRIPTION	DATE	REV.	CHKD.	APVD.
△x1	Revise base on customer's request.(ECR:CO3120434)	2012.09.28	李阮龍	郭素玲	郭遠峰



Circuit diagram

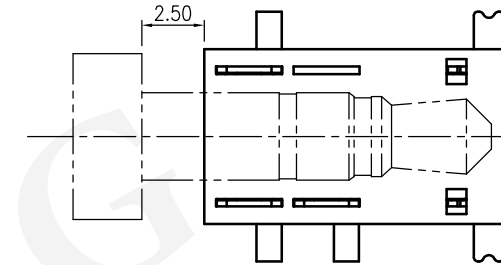


Notes:

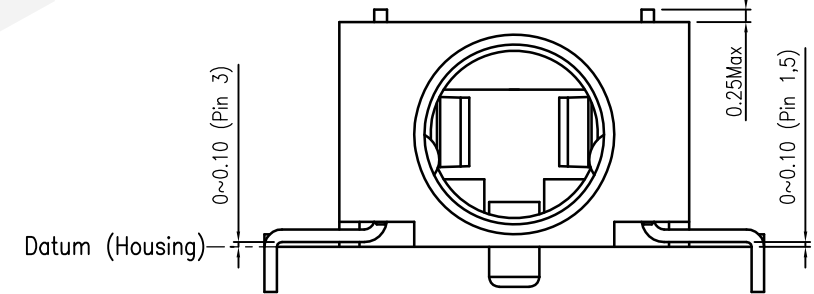
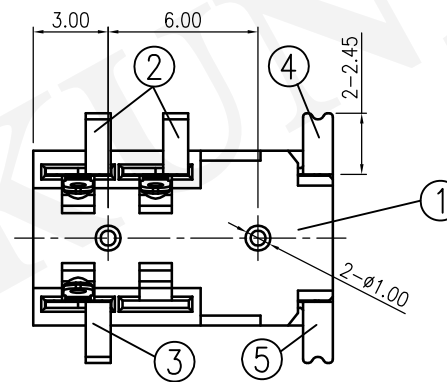
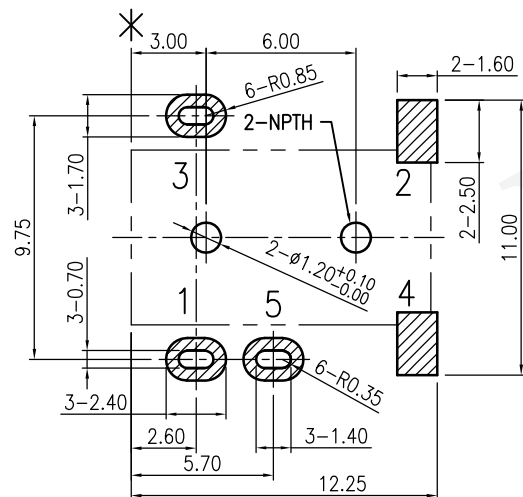
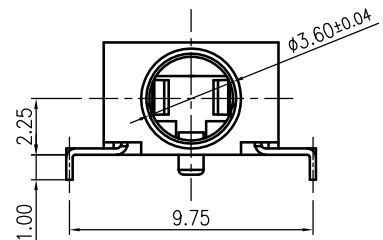
1.Plug position (Schematic drawing 1).

2.Pin 2,4 terminals must keep Max. 0.12 coplanarity.

△3.Pin 1,3,5 terminals (Schematic drawing 2).



Schematic drawing 1



Schematic drawing 2

Scale:2:1

P.C.B layout dimension(Tolerance:±0.05)

(Recommend min. dimension)(Top view)

▨ : Pad Area

----- : Keep Out Area

5	TIP SPRING(4)	1	Copper Alloy	t=0.25	MBNi1 μm-Sn3 μm
4	TIP SPRING(2)	1	Copper Alloy	t=0.25	MBNi1 μm-Sn3 μm
3	SPRING TERMINAL (3)	1	Copper Alloy	t=0.25	MBNi1 μm-Sn3 μm
2	SPRING TERMINAL (1/5)	2	Copper Alloy	t=0.25	MBNi1 μm-Sn3 μm
1	HOUSING	1	High Temperature Thermoplastic UL 94V-0		Black

LTR	PART NAME	Q'TY	MATERIAL	REMARK
120~315	±0.5	DWN	李阮龍	DATE 2011.11.25
30~120	±0.35	DSND	李阮龍	DATE 2011.11.25
6~30	±0.22	CHKD	郭素玲	DATE 2011.11.25
BELOW 6	±0.16	APVD	郭遠峰	DATE 2011.11.25
DIMENSION	TOLERANCE	KUNMING ELECTRONICS CO.,LTD.		
				DWN.NO. A-35003A00BPOT
				1/1 002

SCALE 3.125/1

PROJECTION

UNIT: mm

NAME 3.5mm Miniature Jack

CAT. NO.

KM35003A00BPOT\_

DWN.NO. A-35003A00BPOT

1/1  
002