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1. DDR3 Sync DRAM Features:

Functionality –

- Density: 4G bits
- Organization
  - 32M words x 16 bits x 8 banks
- Package
  - 96-ball FBGA
  - Lead-free (RoHS compliant) and Halogen-free
- Power supply: 1.5V (Typ)
  - VDD, VDDQ=1.5V±0.075V
- Data rate
  - 1866Mbps/1600Mbps/1333Mbps/1066Mb
- 2KB page size
  - Row address: A0 to A14
  - Column address: A0 to A9
- Eight internal banks for concurrent operation
- Burst lengths (BL): 8 and 4 with Burst Chop (BC)
- Burst type (BT):
  - Sequential (8, 4 with BC)
  - Interleave (8, 4 with BC)
- Programable /CAS (Read) Latency (CL)
- Programable /CAS Write Latency (CWL)
- Precharge: auto precharge option for each burst access
- Driver strength: RZQ/7, RZQ/6 (RZQ = 240Ω)
- Refresh: auto-refresh, self-refresh
- Refresh cycles
  - Average refresh period
  - 7.8μs at $0^{O}C \leqq TC \leqq +85^{O}C$
  - 3.9μs at $+85^{O}C < TC \leqq +95^{O}C$
- Operating case temperature range
  - TC = $0^{O}C$ to $+95^{O}C$

Features -

- Double-data-rate architecture: two data transfers per clock cycle
- The high-speed data transfer is realized by the 8 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data and data mask referenced to both edges of DQS
- Data mask (DM) for write data
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- On-Die Termination (ODT) for better signal quality
  - Synchronous ODT
  - Dynamic ODT
  - Asynchronous ODT
- Multi Purpose Register (MPR) for pre-defined pattern read out
- ZQ calibration for DQ drive and ODT
- Programmable Partial Array Self-Refresh (PASR)
- /RESET pin for Power-up sequence and reset function
- SRT range:
  - Normal/extended
- Programmable Output driver impedance control

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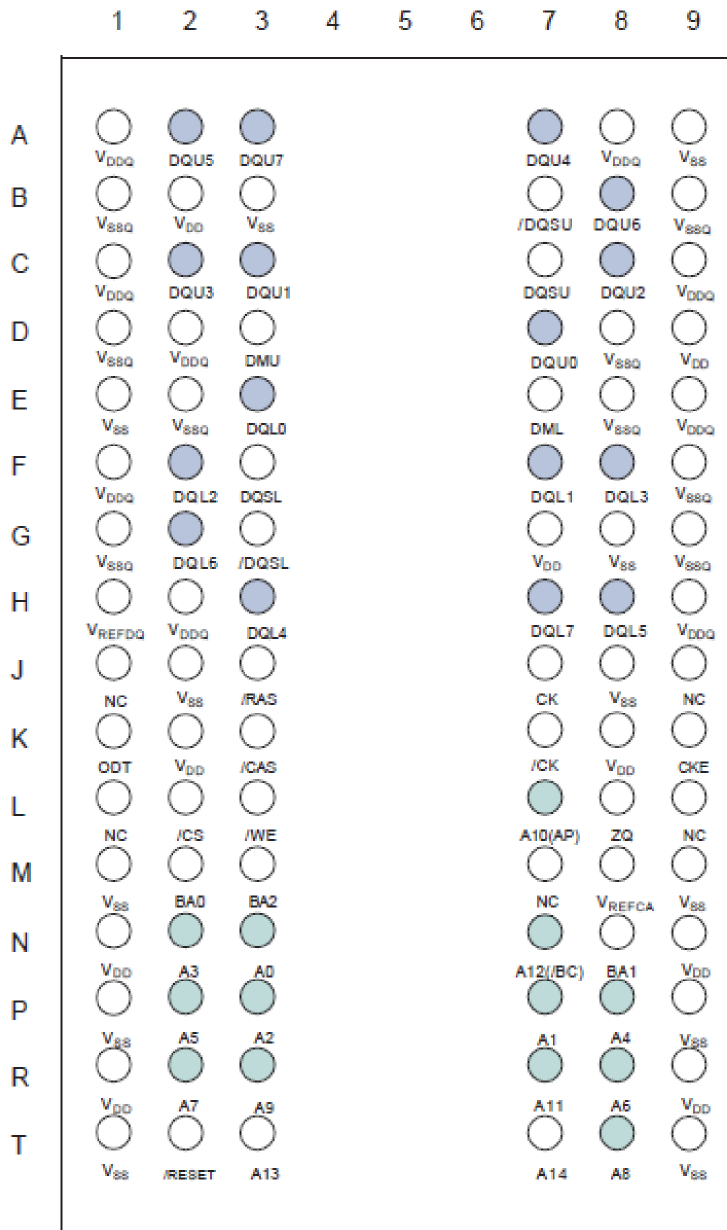
2. Ball Assignments and Descriptions:

96-Ball TFBGA – x16 (Top View)



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Ball Descriptions:

Pin name	Function	Pin name	Pin name
A0 to A14*2	Address inputs A10(AP): Auto precharge A12(/BC): Burst chop	/RESET*2	Active low asynchronous reset
BA0 to BA2*2	Bank select	VDD	Supply voltage for internal circuit
DQU0 to DQU7 DQL0 to DQL7	DQL0 to DQL7	VSS	Ground for internal circuit
DQSU, /DQSU DQSL, /DQSL	Differential data strobe	VDDQ	Supply voltage for DQ circuit
/CS*2	Chip select	VSSQ	Ground for DQ circuit
/RAS, /CAS, /WE*2	Command input	VREFDQ	Reference voltage for DQ
CKE*2	Clock enable	VREFCA	Reference voltage for CA
CK, /CK	Differential clock input	ZQ	Reference pin for ZQ calibration
DMU, DML	Write data mask	NC*1	No connection
ODT*2	Write data mask		

Notes:
1. Not internally connected with die.
2. Input only pins (address, command, CKE, ODT and /RESET) do not supply termination

3. Electrical Conditions:

- All voltages are referenced to VSS (GND)
- Execute power-up and Initialization sequence before proper device operation is achieved.

3.1 Absolute Maximum Ratings

Table 1: Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Power supply voltage	VDD	-0.4 to +1.975	V	1,3
Power supply voltage for output	VDDQ	-0.4 to +1.975	V	1,3
Input voltage	VIN	-0.4 to +1.975	V	1
Output voltage	VOUT	-0.4 to +1.975	V	1
Reference voltage	VREFCA	-0.4 to 0.6 x VDD	V	3
Reference voltage for DQ	VREFDQ	-0.4 to 0.6 x VDDQ	V	3
Storage temperature	Tstg	-55 to +100	^{O}C	1,2
Power dissipation	PD	1.0	W	1
Short circuit output current	IOUT	5.0	W	1

Notes:
1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

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2. Storage temperature is the case surface temperature on the center/top side of the DRAM.
3. VDD and VDDQ must be within 300mV of each other at all times; and VREF must be no greater than 0.6 X VDDQ, When VDD and VDDQ are less than 500mV; VREF may be equal to or less than 300mV.

Caution: Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

3.2 Operating Temperature Condition

Table 2: Operating Temperature Condition

Parameter	Parameter	Rating	Rating	Notes
Operating case temperature	TC	0 to +95	°C	1, 2, 3

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 C to +85 C under all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between +85 C and +95 C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9 s. (This double refresh requirement may not apply for some devices.)
   b) If Self-refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 bit [A6, A7] = [0, 1]) or enable the optional Auto Self-Refresh mode (MR2 bit [A6, A7] = [1, 0]).

3.3 Recommended DC Operating Conditions

Table 3: Recommended DC Operating Conditions (TC = 0°C to +95°C), DDR3 Operation.

Parameter	Symbol	min	typ	max	Unit	Note
Supply voltage	VDD	1.425	1.5	1.575	V	1,2
Supply voltage for DQ	VDDQ	1.425	1.5	1.575	V	1,2

Notes:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3.4 IDD and IDDQ Measurement Conditions

In this chapter, IDD and IDDQ measurement conditions such as test load and patterns are defined. The figure Measurement Setup and Test Load for IDD and IDDQ Measurements shows the setup and test load for IDD and IDDQ measurements.

• IDD currents (such as IDD0, IDD1, IDD2N, IDD2NT, IDD2P0, IDD2P1, IDD2Q, IDD3N, IDD3P, IDD4R, IDD4W, IDD5B, IDD6, IDD6ET and IDD7) are measured as time-averaged currents with all VDD balls of the DDR3 SDRAM under test tied together. Any IDDQ current is not included in IDD currents.
• IDDQ currents (such as IDDQ2NT and IDDQ4R) are measured as time-averaged currents with all VDDQ balls of the DDR3 SDRAM under test tied together. Any IDD current is not included in IDDQ currents.
Note:IDDQ values cannot be directly used to calculate I/O power of the DDR3 SDRAM. They can be used to support correlation of simulated I/O power to actual I/O power as outlined in correlation from simulated channel I/O power to actual channel I/O power supported by IDDQ measurement.
For IDD and IDDQ measurements, the following definitions apply:
• L and 0: VIN ≤ VIL(AC)max
• H and 1: VIN ≥ VIH(AC)min

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• MID-LEVEL: defined as inputs are VREF = VDDQ / 2
• FLOATING: don't care or floating around VREF.
• Timings used for IDD and IDDQ measurement-loop patterns are provided in Timings used for IDD and IDDQ Measurement-Loop Patterns table.
• Basic IDD and IDDQ measurement conditions are described in Basic IDD and IDDQ Measurement Conditions table.
Note: The IDD and IDDQ measurement-loop patterns need to be executed at least one time before actual IDD or IDDQ measurement is started.
• Detailed IDD and IDDQ measurement-loop patterns are described in IDD0 Measurement-Loop Pattern table through IDD7 Measurement-Loop Pattern table.
• IDD Measurements are done after properly initializing the DDR3 SDRAM. This includes but is not limited to setting.
RON = RZQ/7 (34Ω in MR1);
Qoff = 0B (Output Buffer enabled in MR1);
RTT_Nom = RZQ/6 (40Ω in MR1);
RTT_WR = RZQ/2 (120Ω in MR2);
TDQS Feature disabled in MR1
• Define D = {/CS, /RAS, /CAS, /WE}: = {H, L, L, L }
• Define /D = {/CS, /RAS, /CAS, /WE}: = {H, H, H, H }

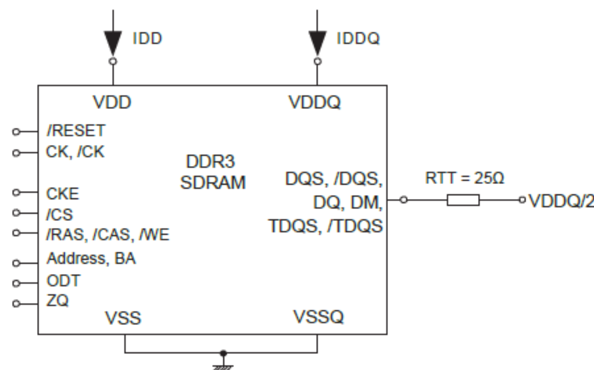

Figure 1: Measurement Setup and Test Load for IDD and IDDQ Measurements

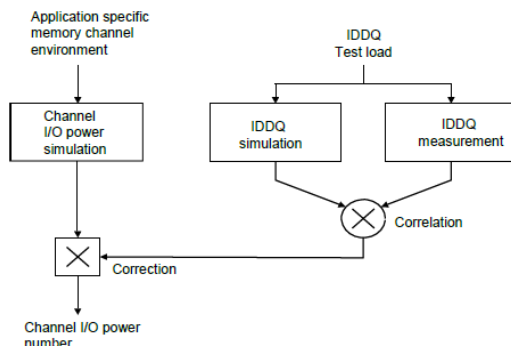

Figure 2: Correlation from Simulated Channel I/O Power to Actual Channel I/O Power Supported by IDDQ Measurement

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3.4.1 Timings Used for IDD and IDDQ Measurement-Loop Patterns

Table 4: Timings Used for IDD and IDDQ Measurement-Loop Patterns

	DDR3-1066	DDR3-1333	DDR3-1600	DDR3-1866	
Parameter	**7-7-7**	**9-9-9**	**11-11-11**	**13-13-13**	**Uni**
CL	7	9	11	13	nCK
tCK(min)	1.875	1.5	1.25	1.071	ns
nRCD(min)	7	9	11	13	nCK
nRC(min)	27	33	39	45	nCK
nRAS(min)	20	24	28	32	nCK
nRP(min)	7	9	11	13	nCK
nFAW	27	30	32	33	nCK
nRRD	6	5	6	6	nCK
nRFC	139	174	208	243	nCK

3.4.2 Basic IDD and IDDQ Measurement Conditions

Table 5: Basic IDD and IDDQ Measurement Conditions

Parameter	Symbol	Description
Operating one bank active Precharge current	IDD0	CKE: H; External clock: on; tCK, nRC, nRAS, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between ACT and PRE; Command, address, bank address inputs: partially toggling according to Table 6; Data I/O: MID-LEVEL; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 7); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; Pattern details: see Table 6
Operating one bank active-read-precharge current	IDD1	CKE: H; External clock: On; tCK, nRC, nRAS, nRCD, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between ACT, RD and PRE; Command, address, bank address inputs, data I/O: partially toggling according to Table 7; DM: stable at 0; Bank activity: cycling with one bank active at a time: 0,0,1,1,2,2,... (see Table 7); Output buffer and RTT: enabled in MR*2; ODT Signal: stable at 0; Pattern details: see Table 7
Precharge standby current	IDD2N	CKE: H; External clock: on; tCK, CL: see Table 4 BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in mode registers*2; ODT signal: stable at 0; pattern details: see Table 8
Precharge standby ODT current	IDD2NT	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 9; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: toggling according to Table 9; pattern details: see Table 9
Precharge standby ODT IDDQ current	IDDQ2NT	Same definition like for IDD2NT, however measuring IDDQ

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		current instead of IDD current
Precharge power-down current slow exit	IDD2P0	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks closed; output buffer and RTT: EMR*2; ODT signal: stable at 0; precharge power down mode: slow exit*3
Precharge power-down current fast exit	IDD2P1	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; precharge power down mode: fast exit*3
Precharge quiet standby current	IDD2Q	CKE: H; External clock: On; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: stable at 0; data I/O: MID-LEVEL; DM: stable at 0;bank activity: all banks closed; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Active standby current	IDD3N	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address Inputs: partially toggling according to Table 8; data I/O: MID-LEVEL; DM: stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 8
Active power-down current	IDD3P	CKE: L; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: stable at 1; Command, address, bank address inputs: stable at 0; data I/O: MID-LEVEL; DM:stable at 0; bank activity: all banks open; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0
Operating burst read current	IDD4R	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1, *6; AL: 0; /CS: H between RD; Command, address, bank address Inputs: partially toggling according to Table 10; data I/O: seamless read data burst with different data between one burst and the next one according to Table 10; DM: stable at 0; bank activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... (see Table 10); Output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 10
Operating burst read IDDQ current	IDDQ4R	Same definition like for IDD4R, however measuring IDDQ current instead of IDD current
Operating burst write current	IDD4W	CKE: H; External clock: on; tCK, CL: see Table 4; BL: 8*1; AL: 0; /CS: H between WR; command, address, bank address inputs: partially toggling according to Table 11; data I/O: seamless write data burst with different data between one burst and the next one according to IDD4W Measurement-Loop Pattern table; DM: stable at 0; bank activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,.. (see Table 11); Output buffer and RTT: enabled in MR*2; ODT signal: stable at H; pattern details:

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		see Table 1
Burst refresh current	IDD5B	CKE: H; External clock: on; tCK, CL, nRFC: see Table 4; BL: 8*1; AL: 0; /CS: H between REF; Command, address, bank address Inputs: partially toggling according to Table 12; data I/O: MID-LEVEL; DM: stable at 0; bank activity: REF command every nRFC (Table 12); output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 12
Self-refresh current: normal temperature range	IDD6	TC: 0 to 85°C; ASR: disabled*4; SRT: Normal*5; CKE: L; External clock: off; CK and /CK: L; CL: see Table 4; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Self-refresh current: extended temperature range	IDD6ET	TC: 0 to 95°C; ASR: Disabled*4; SRT: Extended*5; CK E: L; External clock: off; CK and /CK: L; CL: Table 4; BL: 8*1; AL: 0; /CS, command, address, bank address, data I/O: MID-LEVEL; DM: stable at 0; bank activity: Extended temperature self-refresh operation; output buffer and RTT: enabled in MR*2; ODT signal: MID-LEVEL
Operating bank interleave read current	IDD7	CKE: H; External clock: on; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: see Table 4; BL: 8*1, *6; AL: CL-1; /CS: H between ACT and RDA; Command, address, bank address Inputs: partially toggling according to Table 13; data I/O: read data bursts with different data between one burst and the next one according to Table 13; DM: stable at 0; bank activity: two times interleaved cycling through banks (0, 1, …7) with different addressing, see Table 14; output buffer and RTT: enabled in MR*2; ODT signal: stable at 0; pattern details: see Table 13
RESET low current	IDD8	/RESET: low; External clock: off; CK and /CK: low; CKE: FLOATING; /CS, command, address, bank address, Data IO: FLOATING; ODT signal: FLOATING RESET low current reading is valid once power is stable and /RESET has been low for at least 1ms.

Notes:
1. Burst Length: BL8 fixed by MRS: MR0 bits [1,0] = [0,0].
2. MR: Mode Register
   Output buffer enable: set MR1 bit A12 = 1 and MR1 bits [5, 1] = [0,1];
   RTT_Nom enable: set MR1 bits [9, 6, 2] = [0, 1, 1]; RTT_WR enable: set MR2 bits [10, 9] = [1,0].
3. Precharge power down mode: set MR0 bit A12= 0 for Slow Exit or MR0 bit A12 = 1 for fast exit.
4. Auto self-refresh (ASR): set MR2 bit A6 = 0 to disable or 1 to enable feature.
5. Self-refresh temperature range (SRT): set MR0 bit A7= 0 for normal or 1 for extended temperature range.
6. Read burst type: nibble sequential, set MR0 bit A3 = 0

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Table 6: IDD0 Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11~ Am	A10	A7~ A9	A3~ A6	A0~ A2	Data *2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	
			3,4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	
			…	Repeat pattern 1…4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	
			…	Repeat pattern 1...4 until nRC – 1, truncate if necessary												
			1 x nRC +0	ACT	0	0	1	1	0	0	0	0	0	F	0	
			1 x nRC +1.2	D, D	1	0	0	0	0	0	0	0	0	F	0	
			1 x nRC +3.4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
			…	Repeat pattern nRC + 1,...,4 until 1 × nRC + nRAS – 1, truncate if necessary												
			1 × nRC + nRAS	PRE	0	0	1	0	0	0	0	0	0	F	0	
			…	Repeat nRC + 1,...,4 until 2 × nRC – 1, truncate if necessary												
		1	2 x nRC	Repeat Sub-Loop 0, use BA= 1 instead												
		2	4 x nRC	Repeat Sub-Loop 0, use BA= 2 instead												
		3	6 x nRC	Repeat Sub-Loop 0, use BA= 3 instead												
		4	8 x nRC	Repeat Sub-Loop 0, use BA= 4 instead												
		5	10xnRC	Repeat Sub-Loop 0, use BA= 5 instead												
		6	12xnRC	Repeat Sub-Loop 0, use BA= 6 instead												
		7	14xnRC	Repeat Sub-Loop 0, use BA= 7 instead												

Notes:

1. DM must be driven low all the time. DQS, /DQS are FLOATING
2. DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 7: IDD1 Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 ~Am	A10	A7~ A9	A3~ A6	A0~ A2	Data*2
Toggling	Static H	0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	
			1,2	D, D	1	0	0	0	0	0	0	0	0	0	0	
			3,4	/D, /D	1	1	1	1	0	0	0	0	0	0	0	
			…	Repeat pattern 1...4 until nRCD – 1, truncate if necessary												
			nRCD	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			…	Repeat pattern 1...4 until nRAS – 1, truncate if necessary												
			nRAS	PRE	0	0	1	0	0	0	0	0	0	0	0	
			…	Repeat pattern 1...4 until nRC – 1, truncate if necessary												
			1 x nRC +0	ACT	0	0	1	1	0	0	0	0	0	F	0	
			1 x nRC +1.2	D, D	1	0	0	0	0	0	0	0	0	F	0	
			1 x nRC +3.4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
			…	Repeat pattern nRC + 1,..., 4 until nRC + nRCD – 1, truncate if necessary												
			1 x nRC + nRCD	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			…	Repeat nRC + 1,...,4 until 2 × nRC – 1, truncate if necessary												
			1 x nRC	PRE	0	0	1	0	0	0	0	0	0	F	0	

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	+ nRAS	
	…	Repeat pattern nRC + 1,..., 4 until 2 x nRC – 1, truncate if necessary
1	2 x nRC	Repeat Sub-Loop 0, use BA= 1 instead
2	4 x nRC	Repeat Sub-Loop 0, use BA= 2 instead
3	6 x nRC	Repeat Sub-Loop 0, use BA= 3 instead
4	8 x nRC	Repeat Sub-Loop 0, use BA= 4 instead
5	10xnRC	Repeat Sub-Loop 0, use BA= 5 instead
6	12xnRC	Repeat Sub-Loop 0, use BA= 6 instead
7	14xnRC	Repeat Sub-Loop 0, use BA= 7 instead

Notes:
1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 8: IDD2N and IDD3N Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 ~Am	A10	A7~ A9	A3~ A6	A0~ A2	Data*2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	
			1,	D	1	0	0	0	0	0	0	0	0	0	0	
			2	/D	1	1	1	1	0	0	0	0	0	F	0	
			3	/D	1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, use BA= 1 instead												
		2	8 to 11	Repeat Sub-Loop 0, use BA= 2 instead												
		3	12 to 15	Repeat Sub-Loop 0, use BA= 3 instead												
		4	16 to 19	Repeat Sub-Loop 0, use BA= 4 instead												
		5	20 to 23	Repeat Sub-Loop 0, use BA= 5 instead												
		6	24 to 27	Repeat Sub-Loop 0, use BA= 6 instead												
		7	28 to 31	Repeat Sub-Loop 0, use BA= 7 instead												

Notes:
1. DM must be driven low all the time. DQS, /DQS are FLOATING.
2. DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 9: IDD2NT and IDDQ2NT Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11 ~Am	A10	A7~ A9	A3~ A6	A0~ A2	Data*2
Toggling	Static H	0	0	D	1	0	0	0	0	0	0	0	0	0	0	
			1,	D	1	0	0	0	0	0	0	0	0	0	0	
			2	/D	1	1	1	1	0	0	0	0	0	F	0	
			3	/D	1	1	1	1	0	0	0	0	0	F	0	
		1	4 to 7	Repeat Sub-Loop 0, but ODT = 0 and BA= 1												
		2	8 to 11	Repeat Sub-Loop 0, but ODT = 0 and BA= 2												
		3	12 to 15	Repeat Sub-Loop 0, but ODT = 0 and BA= 3												
		4	16 to 19	Repeat Sub-Loop 0, but ODT = 0 and BA= 4												
		5	20 to 23	Repeat Sub-Loop 0, but ODT = 0 and BA= 5												
		6	24 to 27	Repeat Sub-Loop 0, but ODT = 0 and BA= 6												
		7	28 to 31	Repeat Sub-Loop 0, but ODT = 0 and BA= 7												

Notes:
1. DM must be driven low all the time. DQS, /DQS are FLOATING.
2. DQ signals are FLOATING.

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3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 10: IDD4R and IDDQ4R Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11~ Am	A10	A7~ A9	A3~ A6	A0~A2	Data [*2]
Toggling	Static H	0	0	RD	0	1	0	1	0	0	0	0	0	0	0	00000000
			1,	D	1	0	0	0	0	0	0	0	0	0	0	
			2,3	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
			4	RD	0	1	0	1	0	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	0	0	0	0	0	F	0	
			6,7	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

Notes:
1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 11: IDD4W Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11~ Am	A10	A7~ A9	A3~ A6	A0~ A2	Data [*2]
Toggling	Static H	0	0	WR	0	1	0	0	1	0	0	0	0	0	0	00000000
			1,	D	1	0	0	0	1	0	0	0	0	0	0	
			2,3	/D, /D	1	1	1	1	1	0	0	0	0	F	0	
			4	RD	0	1	0	0	1	0	0	0	0	F	0	00110011
			5	D	1	0	0	0	1	0	0	0	0	F	0	
			6,7	/D, /D	1	1	1	1	1	0	0	0	0	F	0	
		1	8 to 15	Repeat Sub-Loop 0, but BA= 1												
		2	16 to 23	Repeat Sub-Loop 0, but BA= 2												
		3	24 to 31	Repeat Sub-Loop 0, but BA= 3												
		4	32 to 39	Repeat Sub-Loop 0, but BA= 4												
		5	40 to 47	Repeat Sub-Loop 0, but BA= 5												
		6	48 to 55	Repeat Sub-Loop 0, but BA= 6												
		7	56 to 63	Repeat Sub-Loop 0, but BA= 7												

Notes:
1. DM must be driven low all the time. DQS, /DQS are used according to write commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by write command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

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Table 12: IDD5B Measurement-Loop Pattern

CK, /CK	CKE	Sub-loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11~ Am	A10	A7~ A9	A3~ A6	A0~ A2	Data [*2]
Togging	Static H	0	0	REF	0	0	0	1	0	0	0	0	0	0	0	
			1, 2	D	1	0	0	0	0	0	0	0	0	0	0	
			3, 4	/D, /D	1	1	1	1	0	0	0	0	0	F	0	
		1	5 to 8	Repeat cycles 1...4, but BA= 1												
			9 to 12	Repeat cycles 1...4, but BA= 2												
			13 to 16	Repeat cycles 1...4, but BA= 3												
			17 to 20	Repeat cycles 1...4, but BA= 4												
			21 to 24	Repeat cycles 1...4, but BA= 5												
			25 to 28	Repeat cycles 1...4, but BA= 6												
			29 to 32	Repeat cycles 1...4, but BA= 7												
		2	33 to nRFC – 1	Repeat Sub-Loop 1, until nRFC – 1. Truncate, if necessary.												

Notes:

1. DM must be driven low all the time. DQS, /DQS are FLOATING.
2. DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

Table 13: IDD7 Measurement-Loop Pattern

CK, /CK	CKE	Sub - loopl	Cycle nunber	Com-mand	/CS	/RAS	/CAS	/WE	ODT	BA*3	A11~ Am	A10	A7~ A9	A3~ A6	A0~ A2	Data [*2]
		0	0	ACT	0	0	1	1	0	0	0	0	0	0	0	
			1	RDA	0	1	0	1	0	0	0	1	0	0	0	00000000
			2	D	1	0	0	0	0	0	0	0	0	0	0	
			...	Repeat above D Command until nRRD – 1												
		1	nRRD	ACT	0	0	1	1	0	1	0	0	0	F	0	
			nRRD+1	RDA	0	1	0	1	0	1	0	1	0	F	0	
			nRRD+2	D	1	0	0	0	0	1	0	0	0	F	0	
			...	Repeat above D Command until 2 × nRRD – 1												
		2	2 x nRRD	Repeat Sub-Loop 0, but BA= 2												
		3	3 x nRRD	Repeat Sub-Loop 1, but BA= 3												
		4	4 x nRRD	D	1	0	0	0	0	3	0	0	0	F	0	
				Assert and repeat above D Command until nFAW – 1, if necessary												
		5	nFAW	Repeat Sub-Loop 0, but BA= 4												
		6	nFAW + nRRD	Repeat Sub-Loop 1, but BA= 5												
		7	nFAW +2xnRRD	Repeat Sub-Loop 0, but BA= 6												
		8	nFAW + 3 x nRRD	Repeat Sub-Loop 1, but BA= 7												
		9	nFAW + 4 x nRRD	D	1	0	0	0	0	7	0	0	0	F	0	
				Assert and repeat above D Command until 2 × nFAW – 1, if necessary												
		10	2 x nFAW + 0	ACT	0	0	1	1	0	0	0	0	0	F	0	
		11	2 x nFAW + 1	RDA	0	1	0	1	0	0	0	1	0	F	0	00110011
			2 x nFAW + 2	D	1	0	0	0	0	0	0	0	0	F	0	
				Repeat above D Command until 2 × nFAW + nRRD – 1												
			2 x nFAW + nRRD	ACT	0	0	1	1	0	1	0	0	0	0	0	
			2 x nFAW + nRRD +	RDA	0	1	0	1	0	1	0	1	0	0	0	00000000

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	1												
	2 x nFAW + nRRD + 2	D	1	0	0	0	0	1	0	0	0	0	0
		Repeat above D Command until 2 × nFAW + 2 × nRRD – 1											
12	2 x nFAW +2 x nRRD	Repeat Sub-Loop 10, but BA= 2											
13	2 x nFAW + 3 x nRRD	Repeat Sub-Loop 11, but BA= 3											
14	2 x nFAW + 4 x nRRD	D	1	0	0	0	0	3	0	0	0	0	0
		Assert and repeat above D Command until 3 × nFAW – 1, if necessary											
15	3 x nFAW	Repeat Sub-Loop 10, but BA= 4											
16	3 x nFAW +nRRD	Repeat Sub-Loop 10, but BA= 5											
17	3 x nFAW + 2 x nRRD	Repeat Sub-Loop 10, but BA= 6											
18	3 x nFAW + 3 x nRRD	Repeat Sub-Loop 10, but BA= 7											
18	3 x nFAW + 4 x nRRD	D	1	0	0	0	0	7	0	0	0	0	0
		Assert and repeat above D Command until 4 × nFAW – 1, if necessary											

Notes:

1. DM must be driven low all the time. DQS, /DQS are used according to read commands, otherwise FLOATING.
2. Burst sequence driven on each DQ signal by read command. Outside burst operation, DQ signals are FLOATING.
3. BA: BA0 to BA2.
4. Am: m means Most Significant Bit (MSB) of Row address.

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4. Electrical Specifications:

4.1 DC Characteristics

Table 14: DC Characteristics 1 (VDD, VDDQ = 1.425V to 1.575V)

Parameter	Symbol	Data rate	x16(max)	unit	Notes
Operating current (ACT-PRE)	IDD0	1066	65	mA	
		1333	70		
		1600	75		
		1866	80		
Operating current (ACT-RD-PRE)	IDD1	1066	80	mA	
		1333	85		
		1600	90		
		1866	95		
Precharge power-down standby current	IDD2P1	1066	35	mA	FastPD Exit
		1333	40		
		1600	45		
		1866	50		
	IDD2P0	1066	20	mA	SlowPD Exit
		1333	20		
		1600	20		
		1866	20		
Precharge standby current	IDD2N	1066	50	mA	
		1333	50		
		1600	50		
		1866	50		
Precharge standby ODT current	IDD2NT	1066	50	mA	
		1333	50		
		1600	50		
		1866	55		
Precharge quiet standby current	IDD2Q	1066	45	mA	
		1333	50		
		1600	55		
		1866	60		
Active power-down current (Always fast exit)	IDD3P	1066	40	mA	
		1333	42		
		1600	44		
		1866	53		
Active standby current	IDD3N	1066	55	mA	
		1333	60		
		1600	65		
		1866	75		
Operating current (Burst read operating)	IDD4R	1066	135	mA	
		1333	145		
		1600	155		
		1866	175		
Operating current (Burst write operating)	IDD4W	1066	145	mA	
		1333	155		
		1600	165		
		1866	185		
Burst refresh	IDD5B	1066	250	mA	

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current		1333	250	
		1600	250	
		1866	250	
All bank interleave read current	IDD7	1066	220	mA
		1333	230	
		1600	240	
		1866	260	
RESET low current	IDD8		20	mA

Table 15: Self-Refresh Current (TC = 0°C to +85°C, VDD, VDDQ = 1.425V to 1.575V)

Parameter	Symbol	max	unit	Notes
Self-refresh current normal temperature range	IDD6	18	mA	Max
Self-refresh current extended temperature range	IDD6ET	22	mA	Max@95'C
Self-refresh current Room temperature(25C)	IDD6	7	mA	Typical

4.2 Pin Capacitance

Table 16: Pin Capacitance [DDR3-1066 to 1866] (TC = 25°C, VDD, VDDQ = 1.425V to 1.575V)

		DDR3-1066		DDR3-1333		DDR3-1600		DDR3-1866			
Parameter	Symbol	Min	Max	Min	Max	Min	Max	Min	Max	Units	Notes
Input/output capacitance	CIO	1.4	2.7	1.4	2.5	1.4	2.3	1.4	2.2	pF	1, 2
Input capacitance, CK and /CK	CCK	0.8	1.6	0.8	1.4	0.8	1.4	0.8	1.3	pF	2
Input capacitance delta, CK and /CK	CDCK	0	0.15	0	0.15	0	0.15	0	0.15	pF	2, 3
Input/output capacitance delta, DQS and /DQS	CDDQS	0	0.2	0	0.15	0	0.15	0	0.15	pF	2, 4
Input capacitance, (control, address, command, input-only pins)	CI	0.75	1.35	0.75	1.3	0.75	1.3	0.75	1.2	pF	2, 5
Input capacitance delta, (All control input-only pins)	CDI_CTRL	-0.5	0.3	-0.4	0.2	-0.4	0.2	-0.4	0.2	pF	2, 6, 7
Input capacitance delta, (All addres/command input-only pins)	CDI_ADD_CMD	-0.5	0.5	-0.4	0.4	-0.4	0.4	-0.4	0.4	pF	2, 8, 9
Input/output capacitance delta, DQ,DM, DQS, /DQS, TDQS, /TDQS	CDIO	-0.5	0.3	-0.5	0.3	-0.5	0.3	-0.5	0.3	pF	2, 10
Input/output capacitance of ZQ pin	CZQ	-	3	-	3	-	3	-	3	pF	2, 11

Notes:

1. Although the DM, TDQS and /TDQS pins have different functions, the loading matches DQ and DQS.
2. VDD, VDDQ, VSS, VSSQ applied and all other pins floating (except the pin under test, CKE, /RESET and ODT as necessary). VDD = VDDQ = 1.5V, VBIAS=VDD/2 and ondie termination off.
3. Absolute value of CCK-C/CK.
4. Absolute value of CIO(DQS)-CIO(/DQS).\
5. CI applies to ODT, /CS, CKE, A0-A14, BA0-BA2, /RAS, /CAS and /WE.
6. CDI_CTRL applies to ODT, /CS and CKE.
7. CDI_CTRL = CI(CTRL) – 0.5 × (CI(CK)+CI(/CK)).
8. CDI_ADD_CMD applies to A0-A15, BA0-BA2, /RAS, /CAS and /WE.
9. CDI_ADD_CMD = CI(ADD_CMD) – 0.5 × (CI(CK)+CI(/CK)).
10. CDIO=CIO(DQ,DM) – 0.5 × (CIO(DQS)+CIO(/DQS)).
11. Maximum external load capacitance on ZQ pin: 5pF.

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4.3 Standard Speed Bins

4.4

Table 17: DDR3-1066 Speed Bins

Speed Bin	/CAS write latency	DDR3-1066		Unit	Notes
CL-tRCD-tRP		7-7-7			
Symbol		min	max		
tAA		13.125	20	ns	
tRCD		13.125	—	ns	
tRP		13.125	—	ns	
tRC		50.625	—	ns	
tRAS		37.5	9 x tREFI	ns	
tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	
	CWL=6	Reserved	Reserved	ns	
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	
	CWL=6	Reserved	Reserved	ns	
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	
	CWL=6	1.875	<2.5	ns	
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	
	CWL=6	1.875	<2.5	ns	
Supported CL settings			5, 6, 7, 8	nCK	
Supported CWL settings			5, 6	nCK	

Table 18: DDR3-1333 Speed Bins

Speed Bin	/CAS write latency	DDR3-1333		Unit	Notes
CL-tRCD-tRP		9-9-9			
Symbol		min	max		
tAA		13.5 (13.125)	20	ns	9
tRCD		13.5 (13.125)	—	ns	9
tRP		13.5 (13.125)	—	ns	9
tRC		49.5 (49.125)	—	ns	9
tRAS		36	9 x tREFI	ns	8
tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 6
	CWL=6, 7	Reserved	Reserved	ns	4
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 6
	CWL=6	Reserved	Reserved		4
	CWL=7	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 6
	CWL=7	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5		1, 2, 3, 6
	CWL=7	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3,
tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3,

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Supported CL settings		5, 6, 7, 8, 9, 10		nCK	
Supported CWL settings		5, 6, 7		nCK	

Table 19: DDR3-1600 Speed Bins

Speed Bin	/CAS write latency	DDR3-1600		Unit	Notes
CL-tRCD-tRP		11-11-11			
Symbol		min	max		
tAA		13.75 (13.125)	20	ns	9
tRCD		13.75 (13.125)	—	ns	9
tRP		13.5 (13.125)	—	ns	9
tRC		48.75 (48.125)	—	ns	9
tRAS		35	9 x tREFI	ns	8
tCK(avg)@CL=5	CWL=5	3.0	3.3	ns	1, 2, 3, 7
	CWL=6, 7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 7
	CWL=6	Reserved	Reserved	ns	4
	CWL=7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 7
	CWL=7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 7
	CWL=7, 8	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 7
	CWL=8	Reserved	Reserved	ns	4
tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 7
	CWL=8	Reserved	Reserved	ns	4
tCK(avg)@CL=11	CWL=5, 6, 7	Reserved	Reserved	ns	4
	CWL=8	1.25	<1.5		1, 2, 3
Supported CL settings		5, 6, 7, 8, 9, 10, 11		ns nCK	
Supported CWL settings		5, 6, 7, 8		nCK	

Table 20: DDR3-1866 Speed Bins

Speed Bin	/CAS write latency	DDR3-1866		Unit	Notes
CL-tRCD-tRP		13-13-13			
Symbol		min	max		
tAA		13.91 (13.125)	20	ns	9
tRCD		13.91 (13.125)	—	ns	9
tRP		13.91 (13.125)	—	ns	9
tRC		47.91 (47.125)	—	ns	9
tRAS		34	9 x tREFI	ns	8
tCK(avg)@CL=6	CWL=5	2.5	3.3	ns	1, 2, 3, 8
	CWL=6	Reserved	Reserved	ns	4

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	CWL=7, 8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=7	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 8
	CWL=7, 8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=8	CWL=5	Reserved	Reserved	ns	4
	CWL=6	1.875	<2.5	ns	1, 2, 3, 8
	CWL=7, 8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=9	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 8
	CWL=8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=10	CWL=5, 6	Reserved	Reserved	ns	4
	CWL=7	1.5	<1.875	ns	1, 2, 3, 8
	CWL=8, 9	Reserved	Reserved	ns	4
tCK(avg)@CL=11	CWL=5, 6, 7	Reserved	Reserved	ns	4
	CWL=8	1.25	<1.5	ns	1, 2, 3, 8
	CWL=9	Reserved	Reserved	ns	4
tCK(avg)@CL=12	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL=9	Reserved	Reserved	ns	4
tCK(avg)@CL=13	CWL=5, 6, 7, 8	Reserved	Reserved	ns	4
	CWL=9	1.07	<1.25	ns	1, 2, 3
Supported CL settings			6, 8, 10, 13, (7), (9), (11)	ns nCK	
Supported CWL settings			5, 6, 7, 8, 9	nCK	

Notes:

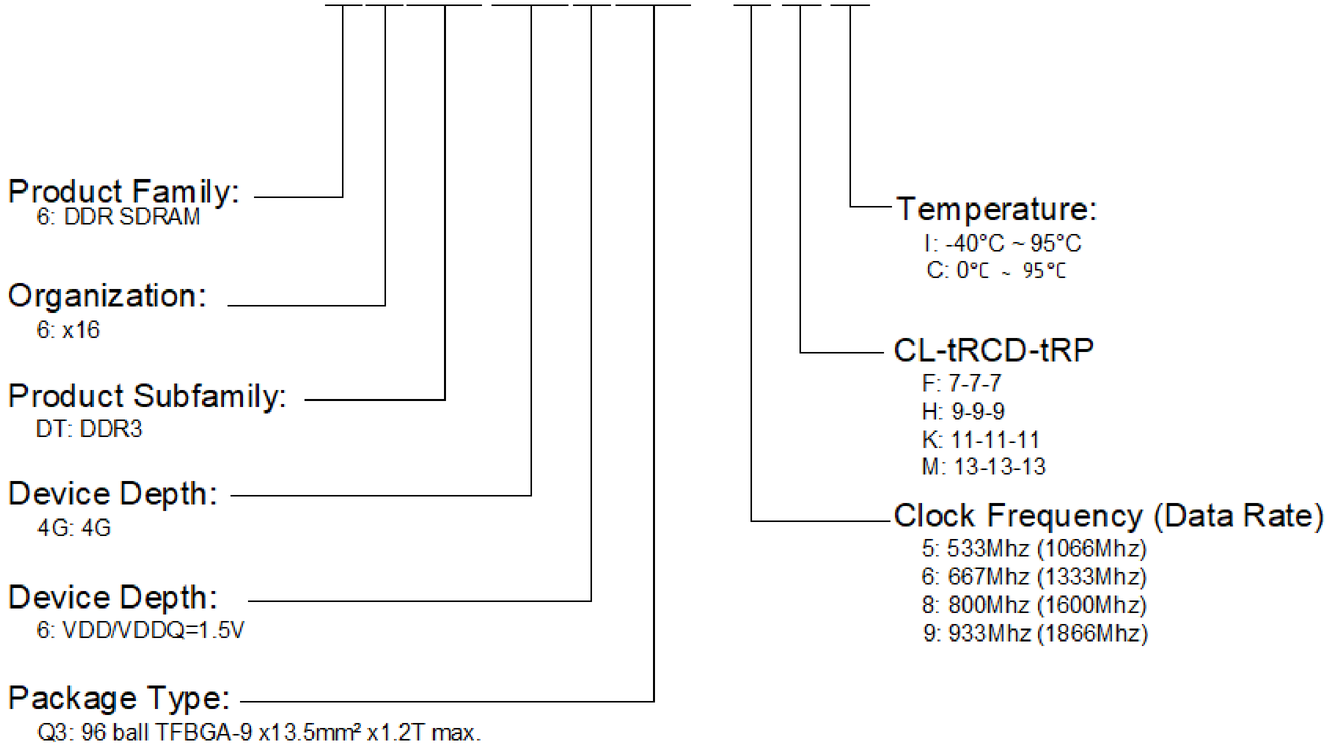
1. The CL setting and CWL setting result in tCK(avg)min and tCK(avg)max requirements. When making a selection of tCK(avg), both need to be fulfilled: Requirements from CL setting as well as requirements from CWL setting.
2. tCK(avg)min limits: Since /CAS latency is not purely analog - data and strobe output are synchronized by the DLL – all possible intermediate frequencies may not be guaranteed. An application should use the next smaller JEDEC standard tCK(avg) value (3.0, 2.5, 1.875, 1.5, or 1.25ns) when calculating CL(nCK) = tAA(ns) / tCK(avg)(ns), rounding up to the next 'Supported CL'.
3. tCK(avg)max limits: Calculate tCK(avg) + tAA(max)/CL selected and round the resulting tCK(avg) down to the next valid speed bin (i.e. 3.3ns or 2.5ns or 1.875ns or 1.25ns). This result is tCK(avg)max corresponding to CL selected.
4. Reserved' settings are not allowed. User must program a different value.
5. Any DDR3-1066 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1066 Speed Bins which are not subject to production tests but verified by design/characterization.
6. Any DDR3-1333 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1333 Speed Bins which is not subject to production tests but verified by design/characterization.
7. Any DDR3-1600 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-160 Speed Bins which is not subject to production tests but verified by design/characterization.
8. Any DDR3-1866 speed bin also supports functional operation at lower frequencies as shown in the table DDR3-1866 Speed Bins which is not subject to production tests but verified by design/characterization
9. tREFI depends on operating case temperature (TC).
10. For devices supporting optional down binning to CL = 7 and CL = 9, tAA/tRCD/tRP(min) must be 13.125 ns or lower. SPD settings must be programmed to match.

5. Selection Guide:

Part Number	VDD/VDDQ	I/O Width	Frequency	Data Rate	PKG TYPE
CS66DT4G6Q3-5Fx	1.5V	X16	533Mhz	1066Mbps/pin	96Ball TFBGA
CS66DT4G6Q3-6Hx	1.5V	X16	667Mhz	1333Mbps/pin	96Ball TFBGA
CS66DT4G6Q3-8Kx	1.5V	X16	800Mhz	1600Mbps/pin	96Ball TFBGA
CS66DT4G6Q3-9Mx	1.5V	X16	933Mhz	1866Mbps/pin	96Ball TFBGA

Chiplus reserves the right to change product or specification without notice.

6. Part Numbering System:



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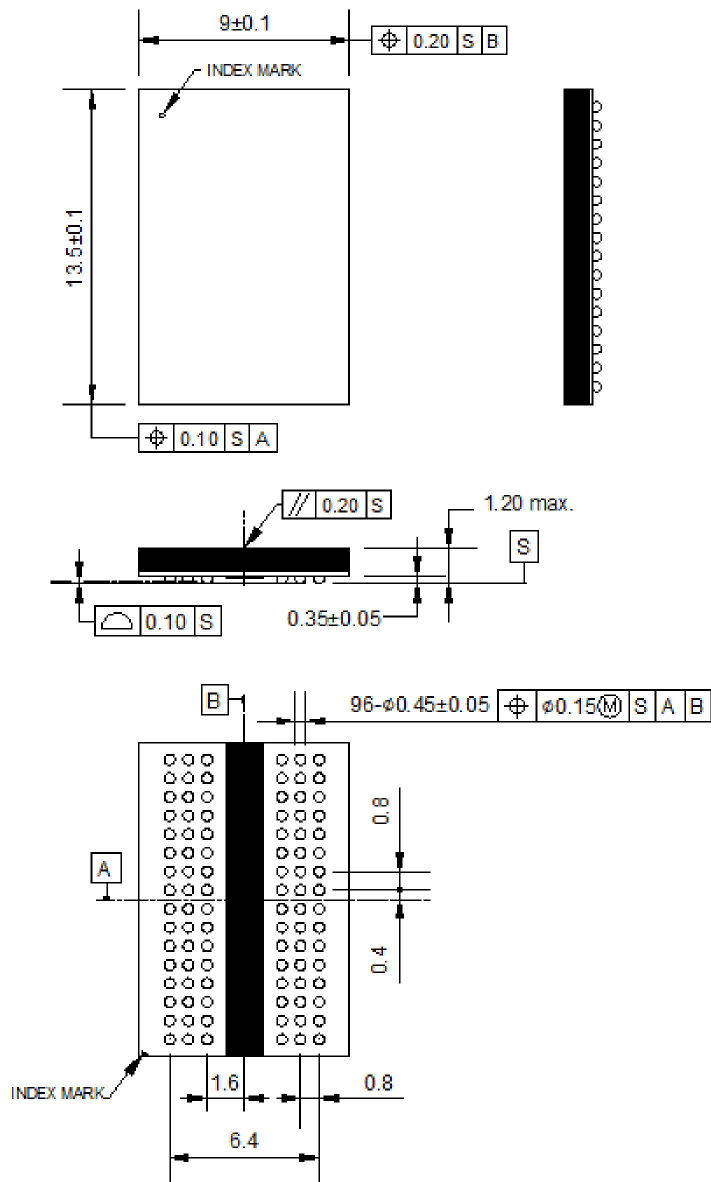
7. Package Outline:

96ball TFBGS- 9x13.5x1.2 mm



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