Rev. No.	History	Issue Date	Remark
1.0	New Issue	May. 22. 2015	

DESCRIPTION

The CS18FS10245 series products are 131,072-words by 8-bits static RAM fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the CS18FS10245 series products exhibit very high-speed performance with single +5-volt power supply while requiring very low power and no clock or refreshing to operate. The CS18FS10245 is packed in a standard 32L SOJ-300mil, 32L STSOP-8x13.4mm, 32L TSOP(I)-8x20mm and 32L PDIP-300mil.

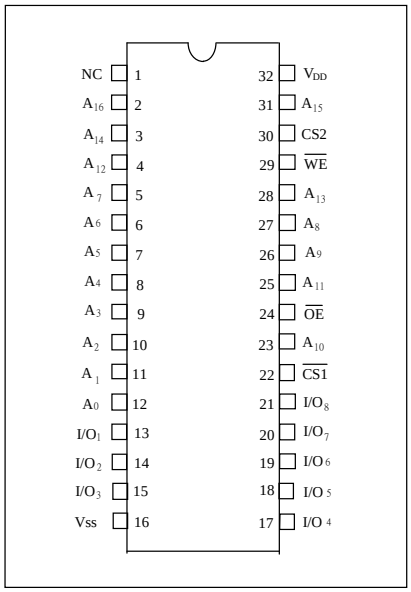
FEATURES

- 131,072-word x 8-bit organization
- Operation voltage: 4.5~5.5V
- Fully static operation - no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
  1. Active: 60/50/45 mA（Max.）
  2. Standby: 500 uA
- Very high speed access: 10/12/15 ns（Max.）
- Output Enable（$\overline{OE}$）available for very fast access

PRODUCT FAMILY

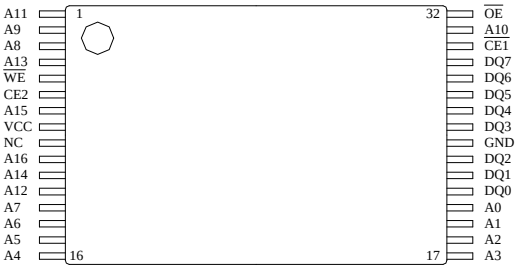
Part No.	Operating Temp	Vcc. Range	Speed (ns)	Supply Current mA (Max.)	Package Type
CS18FS10245	0~70°C	4.5~5.5V	10	60	32L SOJ-300mil 32LSTSOP-8x13.4mm 32L TSOP-8x20mm 32L PDIP-300mil
			12	50	
			15	45	

PIN CONFIGURATIONS



32L SOJ -300 mil

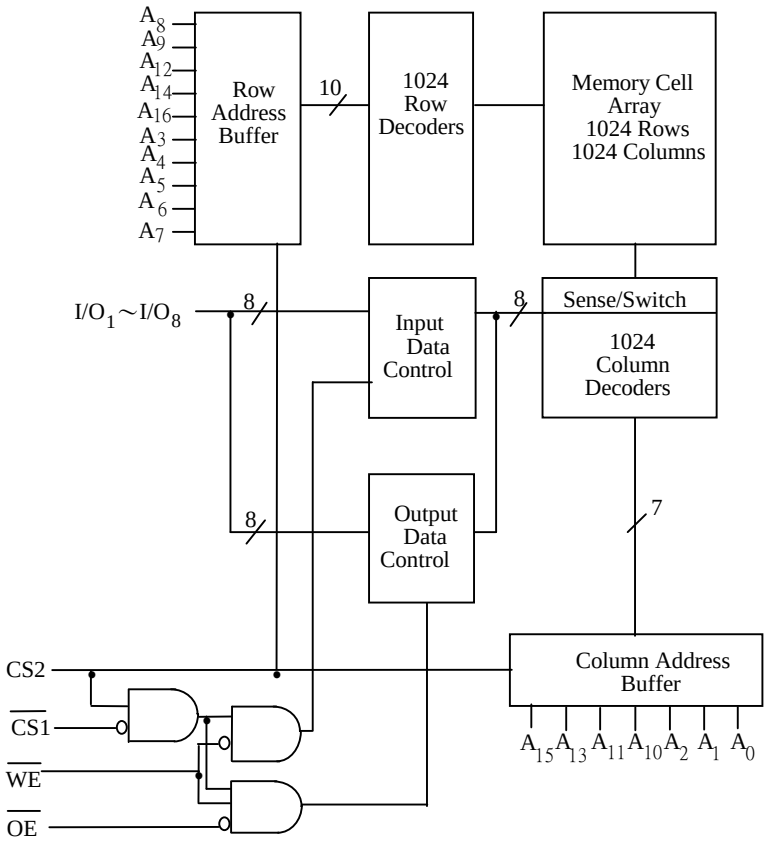
32L PDIP-300 mil



32L TSOP(I)-8x20mm

32L STSOP (I)-8x13.4mm

BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbols	**Functions**
A0~A16	Address Inputs
I/O1～I/O8	Data Inputs / Outputs
$\overline{CS}$1, CS2	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
VDD	Power Supply
VSS	Ground

TRUTH TABLE

$\overline{CS}$	CS2	$\overline{OE}$	$\overline{WE}$	Mode	I/O1～I/O8	VDD Current
H	X	X	X	Not Selected	High Z	Isb, Isb1
X	L	X	X	Not Selected	High Z	Isb, Isb1
L	H	H	H	Output Disable	High Z	IDD
L	H	L	H	Read	Data Out	IDD
L	H	X	L	Write	Data In	IDD

ABSOLUTE MAXIMUM RATINGS

Parameters	Rating	Unit
Supply Voltage to Vss	-0.5 to +7.0	V
Input/Output to Vss	-0.5 to VDD +0.5	V
Allowable Power Dissipation	1.5	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	5V±10%

DC ELECTRICAL CHARACTERISTICS

(VDD = 5V, Vss = 0V, Ta = 0 to 70℃)

Parameters	Symbols	Test Conditions		Min.	Typ.	Max	Unit
Input Low Voltage	V_{IL}	-		-0.3	-	+0.8	V
Input High Voltage	V_{IH}	-		+2.2	-	V_{DD}+0.5	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-5	-	+5	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-5	-	+5	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA	10	-	-	60	mA
		Cycle = MIN	12	-	-	50	mA
		Duty = 100%	15	-	-	45	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle = MIN Duty = 100%		-	-	2	mA
	I_{SB1}	$\overline{CS} \geqq V_{DD}$ -0.2V		-	-	500	uA

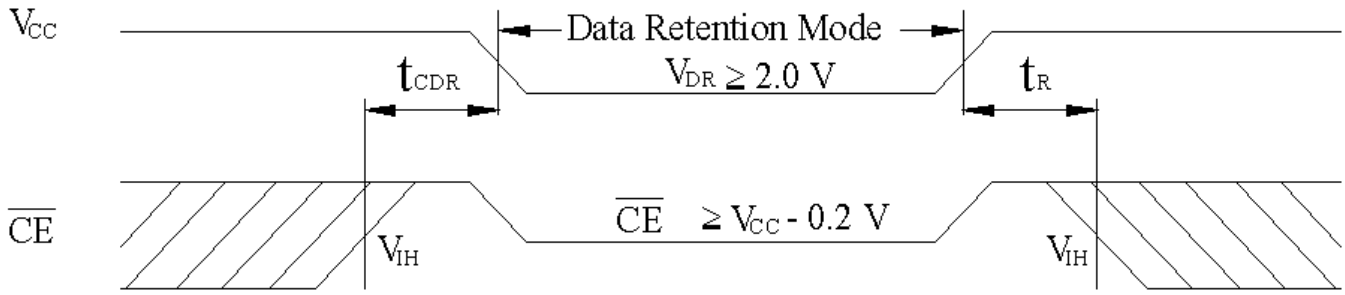
Typical characteristics are measured at VDD = 5V, Ta = 25℃

DATA RETENTION CHARACTERISTICS (TA = 0° ~70°C)

Name	Parameter	Test Condition	MIN	Typ (2)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE≧V_{CC}-0.2V, V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V	2.0			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{CC}=2V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		200	500	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (1)			ns

1. *tRC= .Read Cycle Time.*
2. *TA=25 OC*

LOW Vcc DATA RETENTION WAVEFORM (/CE Controlled)



AC CHARACTERISTICS

Capacitances

(V_{DD} = 5V, Ta = 25℃, f = 1 MHz)

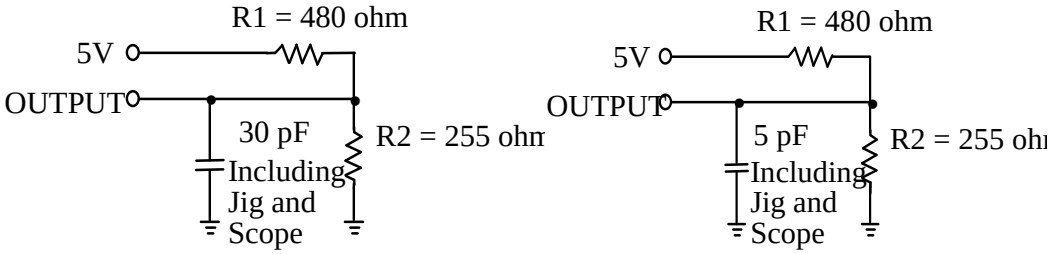
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	5	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	7	pF

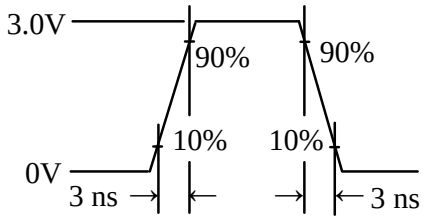
These parameters are sampled but not 100% tested.

AC TEST CONDITIONS

Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	C_L = 30 pF, I_{OH}/I_{OL} = -4 mA / 8 mA

AC TEST LOADS AND WAVEFORMS





(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})

AC PERFORMANCES

(V_{DD} = 5V, V_{SS} = 0V, Ta = 0 to 70℃)

(1) Read Cycle

Parameters	Symbols	CS18FS10245-10		CS18FS10245-12		CS18FS10245-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}	10	-	12	-	15	-	ns
Address Access Time	T_{AA}	-	10	-	12	-	15	ns
Chip Select Access Time	T_{ACS}	-	10	-	12	-	15	ns
Output Enable to Output Valid	T_{AOE}	-	6	-	7	-	8	ns
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	3	-	ns
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	0	-	ns
Chip Deselection to Output in High Z	T_{CHZ}*	-	5	-	6	-	7	ns
Output Disable to Output in High Z	T_{OHZ}*	-	5	-	6	-	7	ns
Output Hold from Address Change	T_{OH}	3	-	3	-	3	-	ns

These parameters are sampled but not 100% tested

(2) Write Cycle

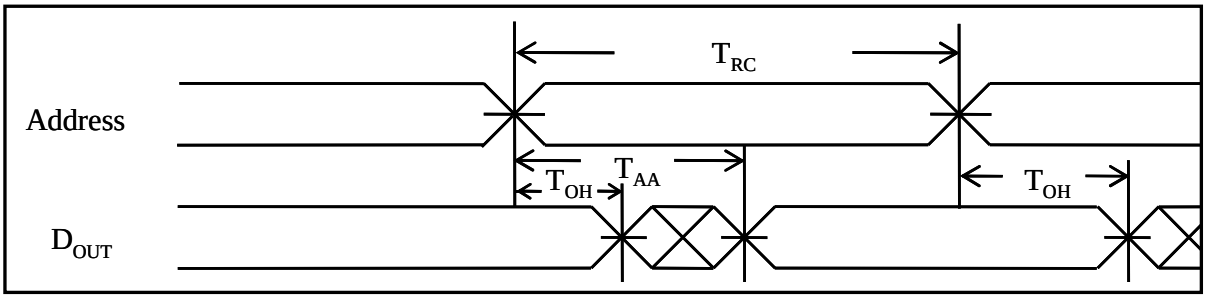
Parameters	Symbols	CS18FS10245-10		CS18FS10245-12		CS18FS10245-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	10	-	12	-	15	-	ns
Chip Selection to End of Write	T_{CW}	8	-	10	-	12	-	ns

Address Valid to End of Write	TAW	8	-	10	-	12	-	ns
Address Setup Time	TAS	0	-	0	-	0	-	ns
Write Pulse Width	TWP	8	-	10	-	12	-	ns
Write Recovery Time	TWR	0	-	0	-	0	-	ns
Data Valid to End of Write	TDW	6	-	8	-	10	-	ns
Data Hold from End of Write	TDH	0	-	0	-	0	-	ns
Write to Output in High Z	TWHZ*	-	5	-	6	-	7	ns
Output Disable to Output in High Z	TOHZ*	-	5	-	6	-	7	ns
Output Active from End of Write	TOW	0	-	0	-	0	-	ns

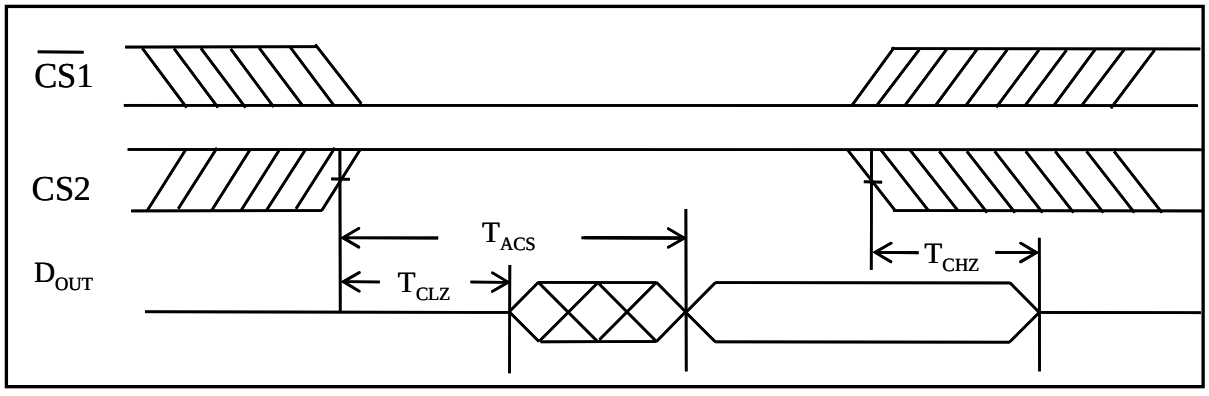
These parameters are sampled but not 100% tested

TIMING WAVEFORMS

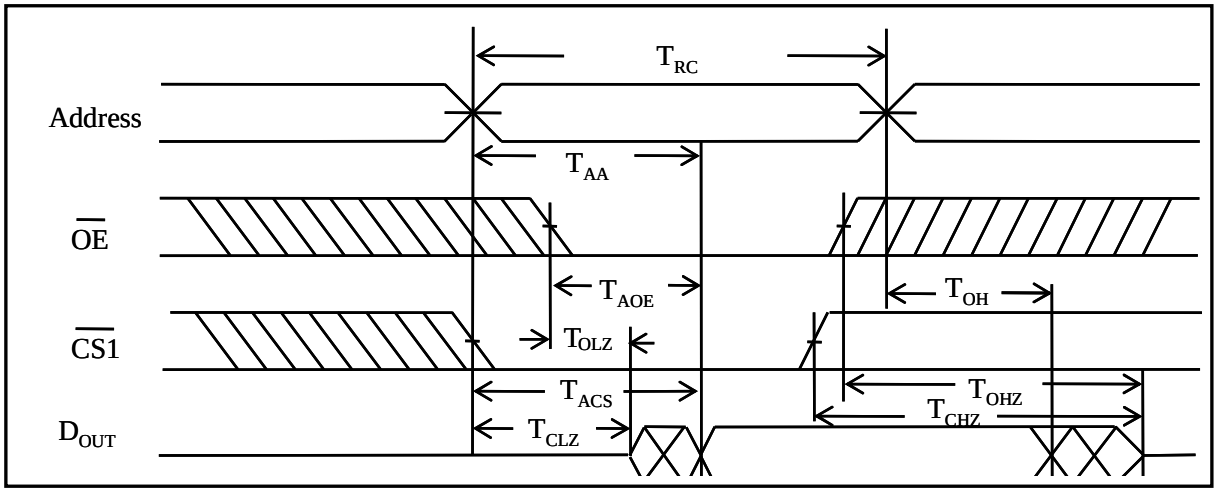
Read Cycle 1 (Address Controlled)



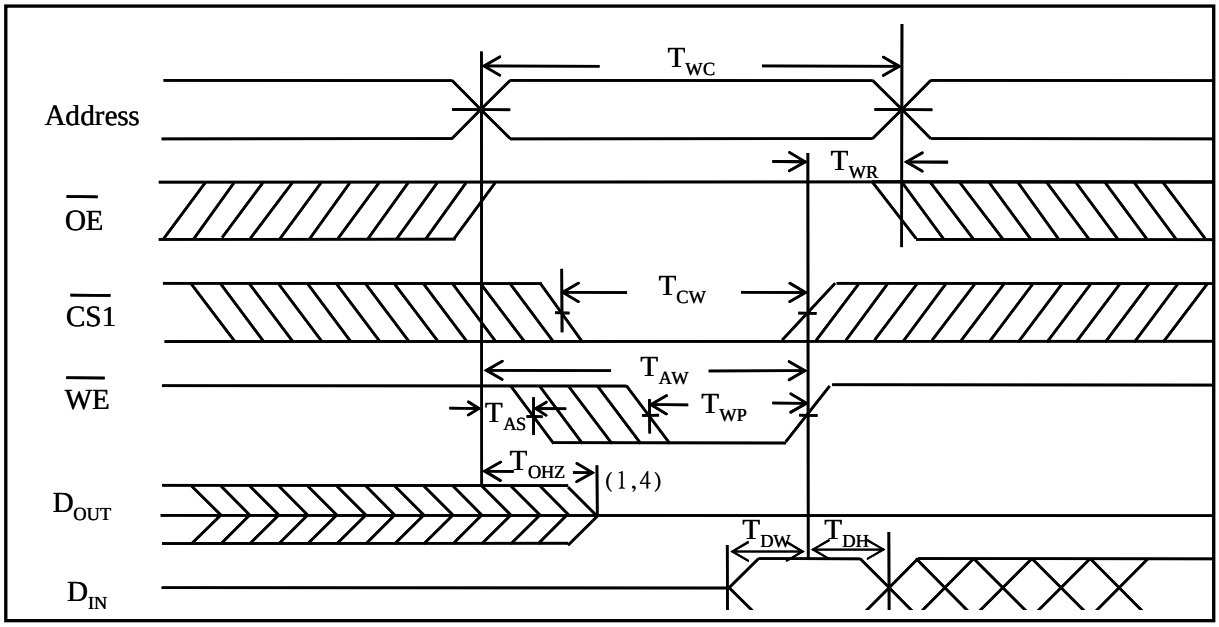
Read Cycle 2 (Chip Select Controlled)



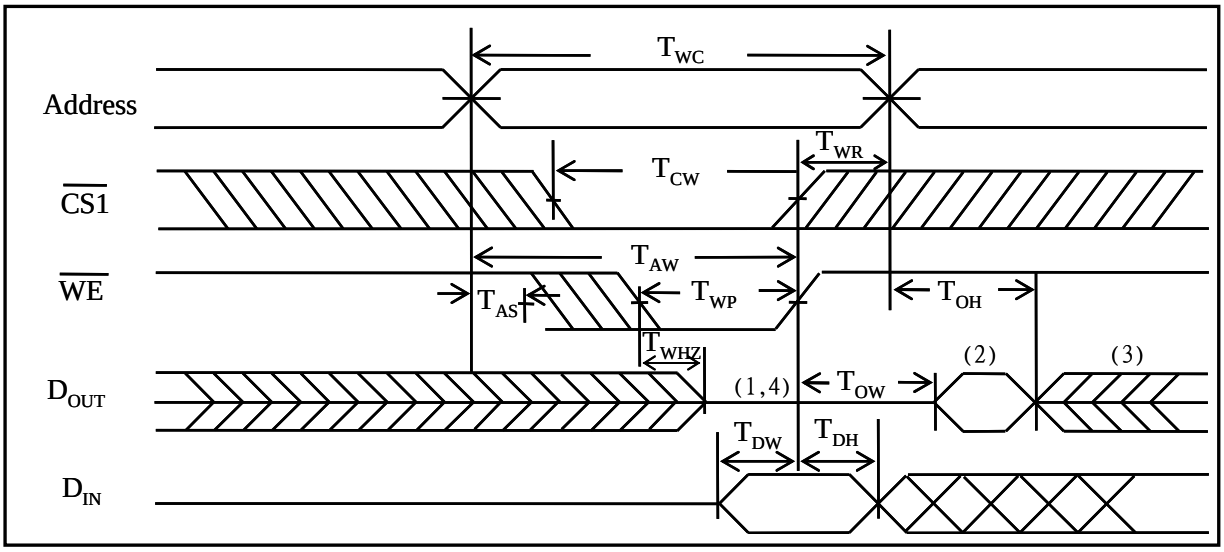
Read Cycle 3 (Output Enable Controlled)



Write Cycle 1 ($\overline{OE}$ Clock)



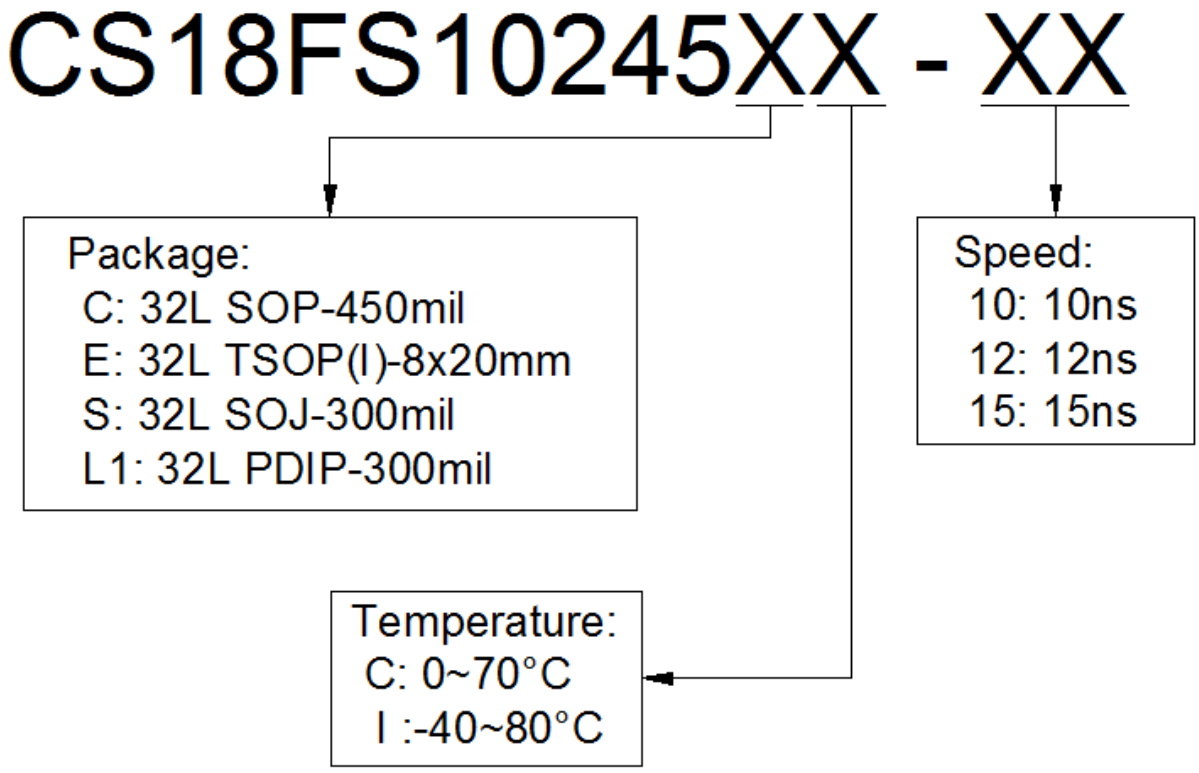
Write Cycle 2 ($\overline{OE}$ = VIL Fixed)



Notes:

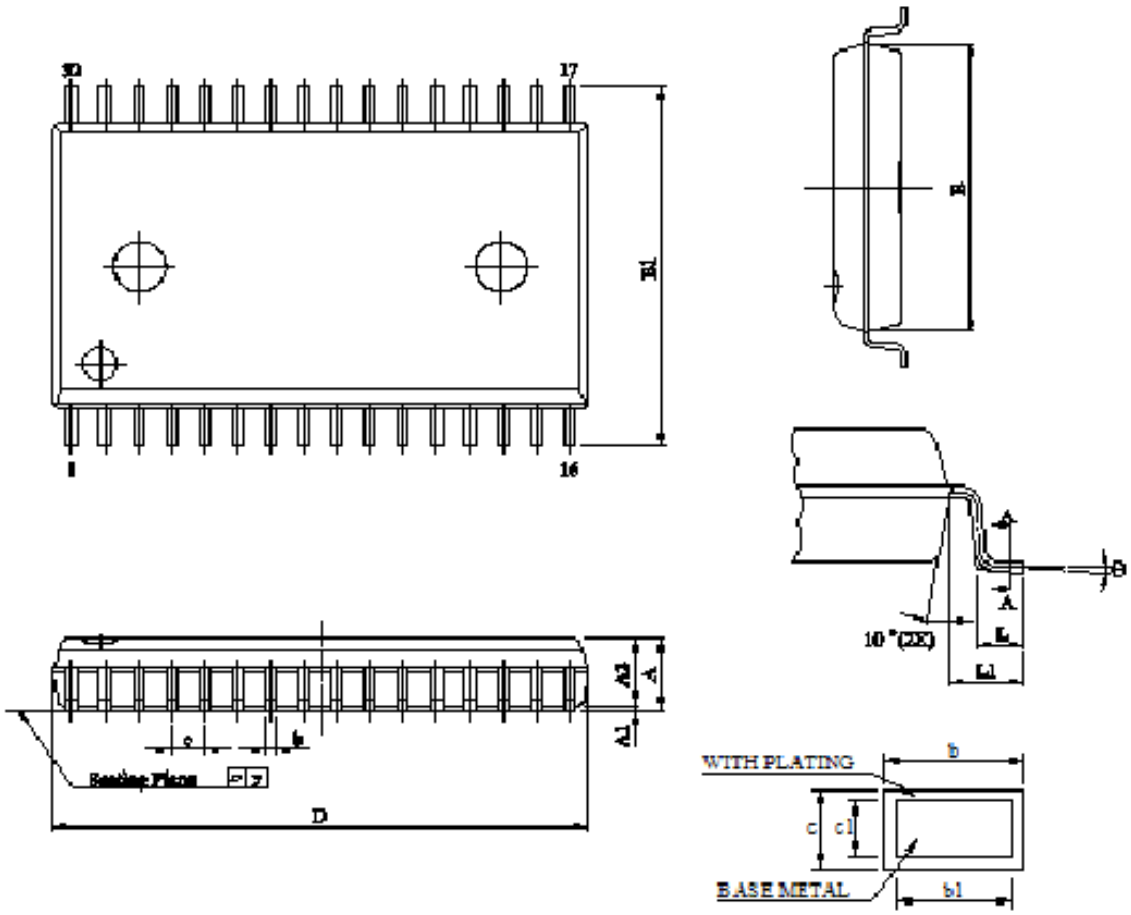
1. *During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.*
2. *The data output from DOUT are the same as the data written to DIN during the write cycle.*
3. *DOUT provides the read data for the next address.*
4. *Transition is measured ±500mV from steady state with CL = 5pF. This parameter is guaranteed but not 100% tested.*

ORDER INFORMATION



PACKAGE OUTLINE

32 SOP - 450 mil

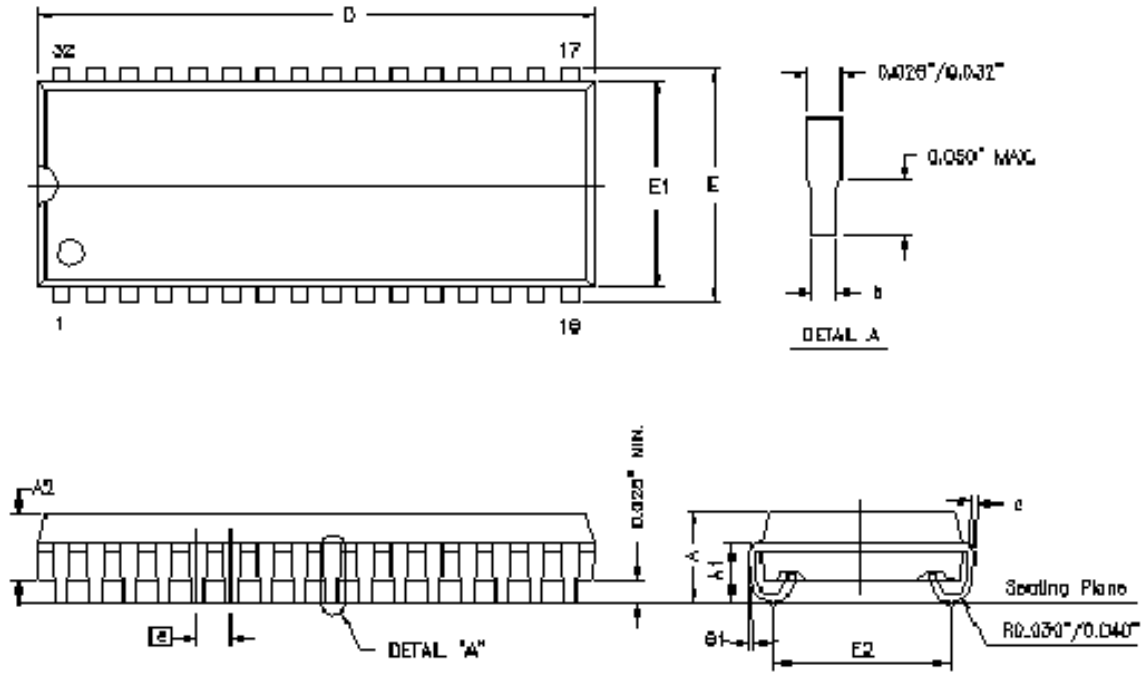


SECTION A-A

Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	e	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	2.645	0.102	2.540	0.35	0.35	0.15	0.15	20.320	11.176	13.792	1.118	0.584	1.194	–	0°
	Nom.	2.821	0.229	2.680	–	–	–	–	20.447	11.303	14.097	1.270	0.834	1.397	–	–
	Max.	2.997	0.356	2.820	0.50	0.46	0.32	0.28	20.574	11.430	14.402	1.422	1.084	1.600	0.1	10°
inch	Min.	0.104	0.004	0.1000	0.014	0.014	0.006	0.006	0.800	0.440	0.543	0.044	0.023	0.047	–	0°
	Nom.	0.111	0.009	0.1055	–	–	–	–	0.805	0.445	0.555	0.050	0.033	0.055	–	–
	Max.	0.118	0.014	0.1110	0.020	0.018	0.012	0.011	0.810	0.450	0.567	0.056	0.043	0.063	0.004	10°

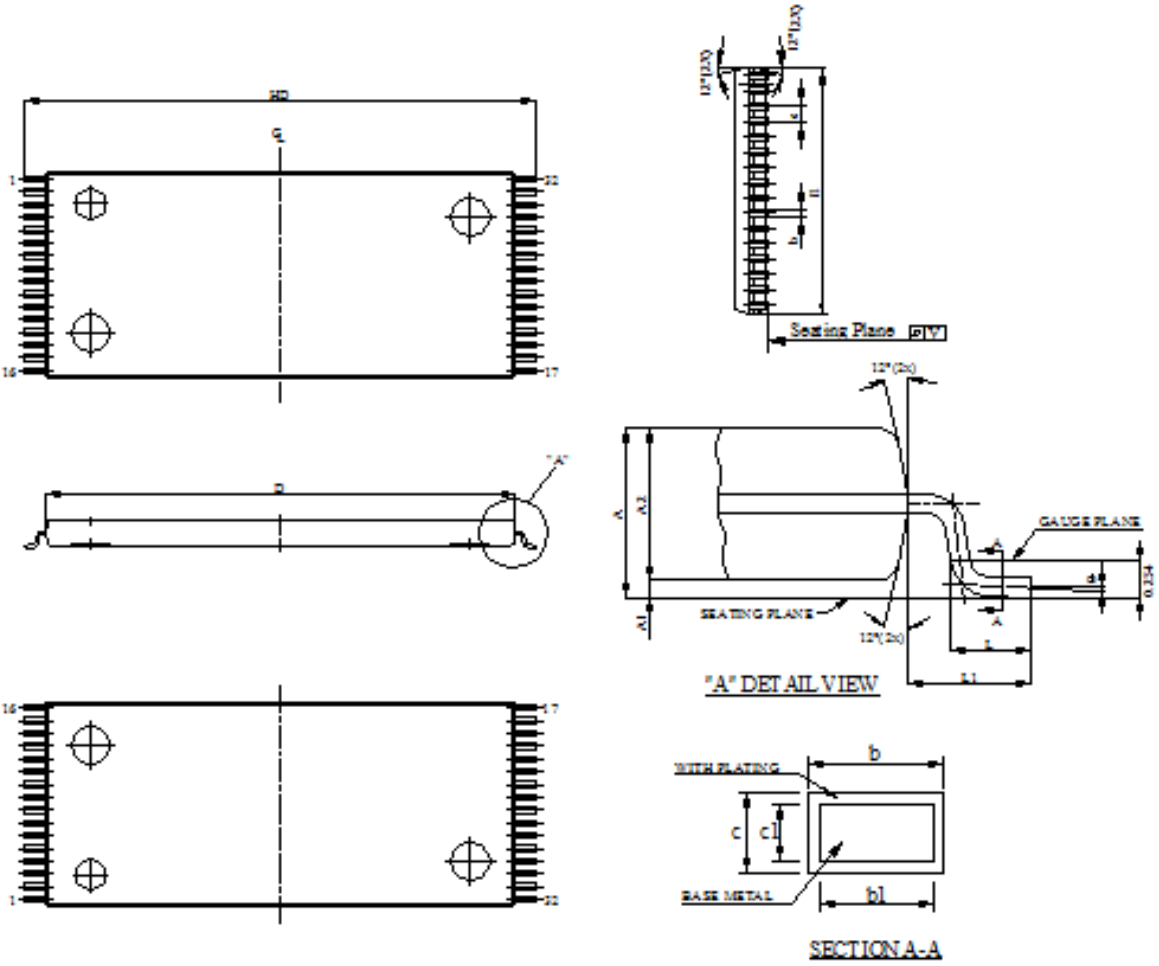
32 SOJ – 300 mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	c	D	E	E1	E2	e	θ
mm	Min.	3.10	2.08	2.41	0.41	0.18	20.83	8.53 bsc	7.49	6.78 bsc	1.27 bsc	0°
	Nom.	3.35	–	2.54	0.46	0.20	20.96		7.62			–
	Max.	3.61	–	2.67	0.51	0.33	21.08		7.75			10°
inch	Min.	0.122	0.082	0.095	0.016	0.007	0.820	0.336 bsc	0.295	0.267 bsc	0.050 bsc	0°
	Nom.	0.132	–	0.100	0.018	0.008	0.825		0.300			–
	Max.	0.142	–	0.105	0.020	0.013	0.830		0.305			10°

32TSOP(I) – 8x20mm



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
mm	Min.	1.00	0.05	0.95	0.17	0.17	0.10	0.10	18.30	7.90	0.40	19.80	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	0.22	0.20	–	–	18.40	8.00	0.50	20.00	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.27	0.23	0.21	0.16	18.50	8.10	0.60	20.20	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.007	0.007	0.004	0.004	0.720	0.311	0.016	0.779	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	0.009	0.008	–	–	0.724	0.315	0.020	0.787	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.011	0.009	0.008	0.006	0.728	0.319	0.024	0.795	0.0277	0.0355	0.004	8°

32PDIP – 300mi