Revision History

Rev. No	History	Issue Date
1.0	New Issue	May. 22,2015

DESCRIPTION

The CS18FS02563 series products are 32,768-words by 8-bits static RAMs fabricated with advanced 8" wafer submicron CMOS technology. Using unique CMOS peripheral circuits and special poly-load 4-transistor memory cells, the CS18FS02563 series products exhibit very high-speed performance with single +3.3-volt power supply while requiring low power and no clock or refreshing to operate. The CS18FS02563 is packed in 28-pin SOP-330mil, 28-pin SOJ-300mil, 28-pin TSOP 1-8x13.4mm and 28-pin PDIP-300mil

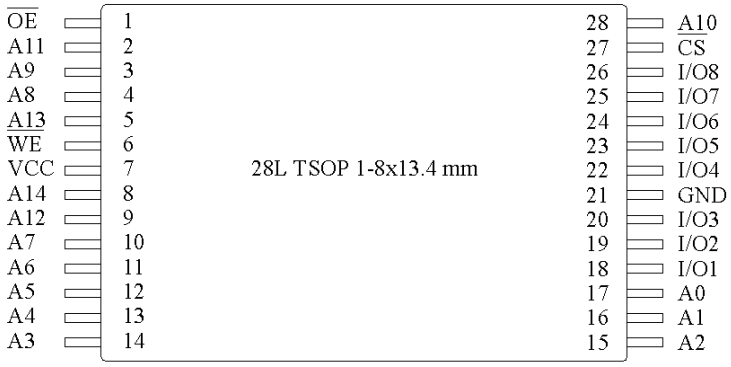
FEATURES

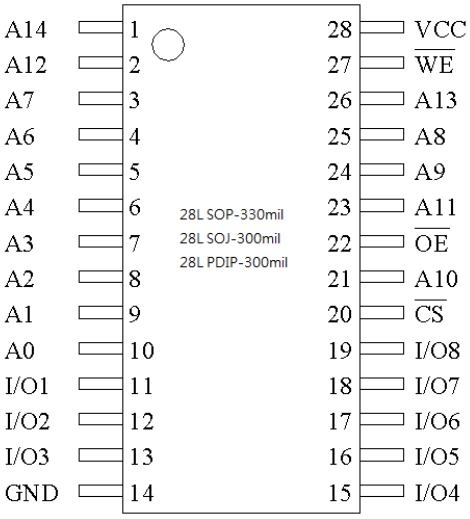
- 32,768-word x 8-bit organization
- Low operation voltage: 3.0~3.6V
- Fully static operation: no clock or refreshing required
- LVTTL-compatible inputs and outputs
- Common I/O capability
- Low power consumption
  1. Active: 100/90 mA (Max.)
  2. Standby: 2 mA
- Very high speed access: 10/12 ns
- Output Enable ($\overline{OE}$) available for very fast access
- Standard pin configuration
  1. 28 SOP - 330mil
  2. 28 TSOP (I) - 8*13.4mm
  3. 28 SOJ - 300mil
  4. 28 PDIP – 300mil

PRODUCT FAMILY

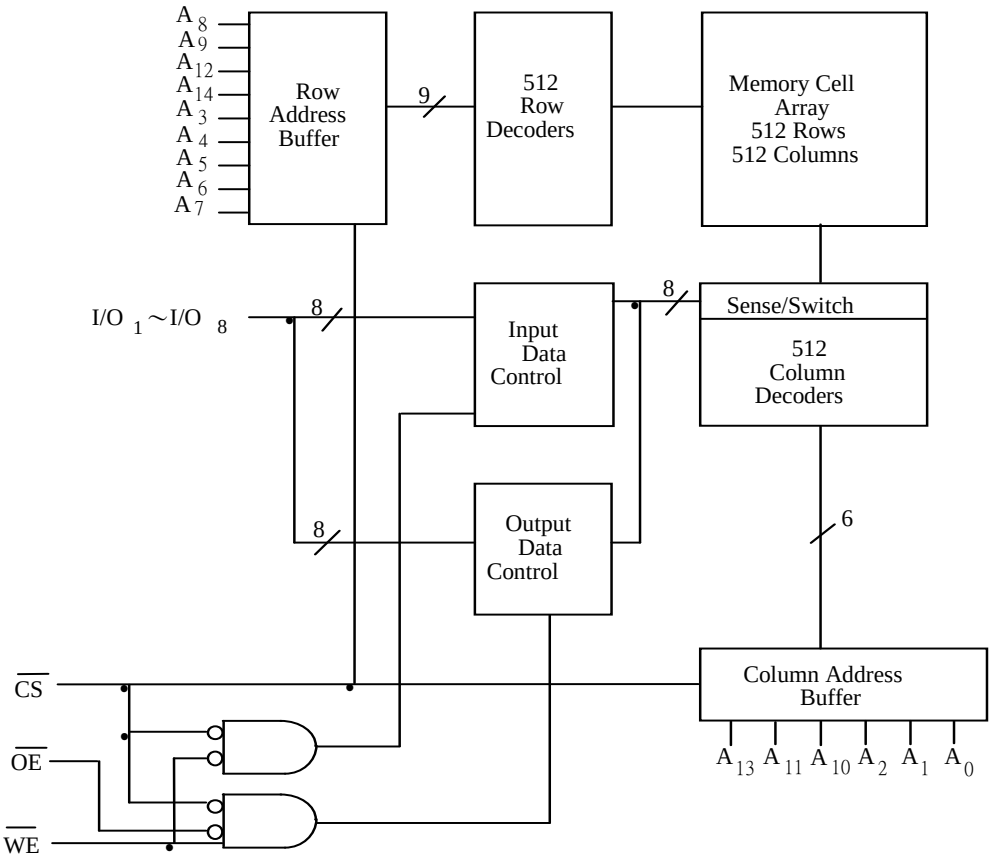
Part No.	Operating Temp	Vcc. Range	Speed (ns)	Supply Current mA (Max.)	Package Type
CS18FS02563	0~70°C	3.0~3.6V	10	100	28 SOP 28 TSOP 28 SOJ 28 PDIP
			12	90	

PIN CONFIGURATIONS





BLOCK DIAGRAM



PIN DESCRIPTIONS

Symbols	Functions
A0~A14	Address Inputs
I/O1~I/O8	Data Inputs / Outputs
$\overline{CS}$	Chip Select Input
$\overline{WE}$	Write Enable Input
$\overline{OE}$	Output Enable Input
V_{DD}	Power Supply
V_{SS}	Ground

TRUTH TABLE

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O1~I/O8	VDD Current
H	X	X	Not Selected	High Z	I_{SB}, I_{SB1}
L	H	H	Output Disable	High Z	I_{DD}
L	L	H	Read	Data Out	I_{DD}
L	X	L	Write	Data In	I_{DD}

ABSOLUTE MAXIMUM RATINGS

Parameters	Rating	Unit
Supply Voltage to V_{SS}	-0.5 to +4.6	V
Input/ Output to V_{SS}	-0.5 to V_{DD} +0.5	V
Allowable Power Dissipation	1.0	W
Storage Temperature	-65 to +150	℃
Operating Temperature	0 to +70	℃

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70ºC	3.3V±5%

DC ELECTRICAL CHARACTERISTICS

(VDD = 3.3V, V_{SS} = 0V, Ta = 0 to 70℃)

Parameters	Symbols	Test Conditions		Min.	Typ.	Max	Unit
Input Low Voltage	V_{IL}	-		-0.3	-	0.8	V
Input High Voltage	V_{IH}	-		2.1	-	V_{DD}+0.3	V
Input Leakage Current	I_{LI}	V_{IN} = V_{SS} to V_{DD}		-10	-	+10	μA
Output Leakage Current	I_{LO}	$V_{I/O}$ = V_{SS} to V_{DD}, $\overline{CS}$ = V_{IH} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL}		-10	-	+10	μA
Output Low Voltage	V_{OL}	I_{OL} = +8.0mA		-	-	0.4	V
Output High Voltage	V_{OH}	I_{OH} = -4.0mA		2.4	-	-	V
Operating Power Supply Current	I_{DD}	$\overline{CS}$ = V_{IL}, I/O = 0 mA Cycle = MIN Duty = 100%	10	-	-	100	mA
			12	-	-	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}$ = V_{IH}, Cycle = MIN Duty = 100%		-	-	15	mA
	I_{SB1}	$\overline{CS}$ ≧ V_{DD} -0.2V		-	-	2	mA

Note: Typical characteristics are measured at VDD = 3.3V, Ta = 25℃

AC CHARACTERISTICS

Capacitances

(V_{DD} = 3.3V, Ta = 25℃, f = 1 MHz)

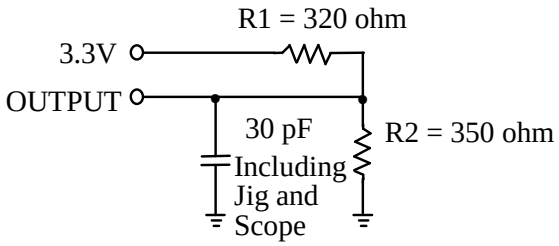
Parameters	Symbols	Conditions	Max.	Unit
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

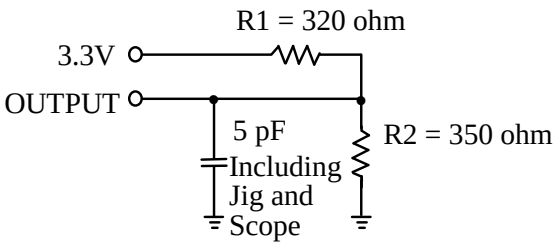
Note: These parameters are sampled but not 100% tested.

AC Test Conditions

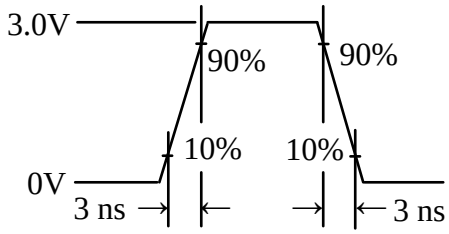
Parameters	Conditions
Input Pulse Levels	0V to 3V
Input Rise and Fall Times	3 ns
Input and Output Timing Reference Level	1.5V
Output Load	CL = 30 pF, I_{OH}/I_{OL} = -4 mA / 8 mA

AC Test Loads and Waveforms





(For T_{CLZ}, T_{OLZ}, T_{CHZ}, T_{OHZ}, T_{WHZ}, T_{OW})



AC PERFORMANCES

(VDD = 3.3V, VSS = 0V, Ta = 0 to 70℃)

(1) Read Cycle

Parameters	Symbols	CS18FS02563-10		CS18FS02563-12		Unit
		Min.	Max.	Min.	Max.	
Read Cycle Time	T_{RC}	10	-	12	-	ns
Address Access Time	T_{AA}	-	10	-	12	ns
Chip Select Access Time	T_{ACS}	-	10	-	12	ns
Output Enable to Output Valid	T_{AOE}	-	6	-	7	ns
Chip Selection to Output in Low Z	T_{CLZ}*	3	-	3	-	ns
Output Enable to Output in Low Z	T_{OLZ}*	0	-	0	-	ns
Chip Deselection to Output in High Z	T_{CHZ}*	-	5	-	6	ns
Output Disable to Output in High Z	T_{OHZ}*	-	5	-	6	ns
Output Hold from Address Change	T_{OH}	3	-	3	-	ns

**These parameters are sampled but not 100% tested*

(2) Write Cycle

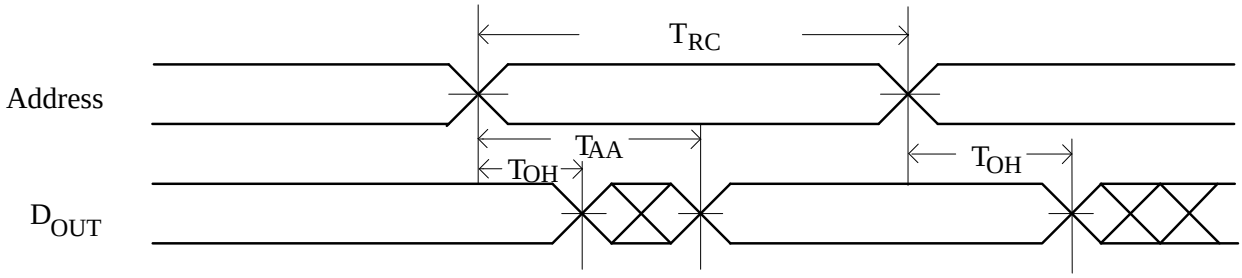
Parameters	Symbols	CS18FS02563-10		CS18FS02563-12		Unit
		Min.	Max.	Min.	Max.	
Write Cycle Time	T_{WC}	10	-	12	-	ns
Chip Selection to End of Write	T_{CW}	8	-	10	-	ns
Address Valid to End of Write	T_{AW}	8	-	10	-	ns
Address Setup Time	T_{AS}	0	-	0	-	ns
Write Pulse Width	T_{WP}	8	-	10	-	ns
Write Recovery Time	T_{WR}	0	-	0	-	ns
Data Valid to End of Write	T_{DW}	6	-	8	-	ns

Data Hold from End of Write	T_{DH}	0	-	0	-	ns
Write to Output in High Z	T_{WHZ*}	-	5	-	6	ns
Output Disable to Output in High Z	T_{OHZ*}	-	5	-	6	ns
Output Active from End of Write	T_{OW}	0	-	0	-	ns

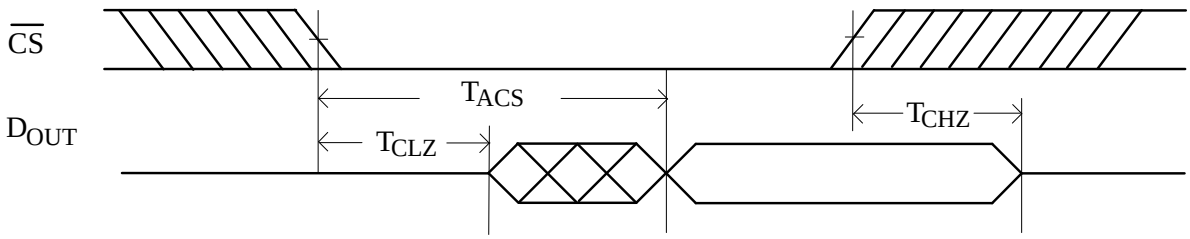
**These parameters are sampled but not 100% tested.*

TIMING WAVEFORMS

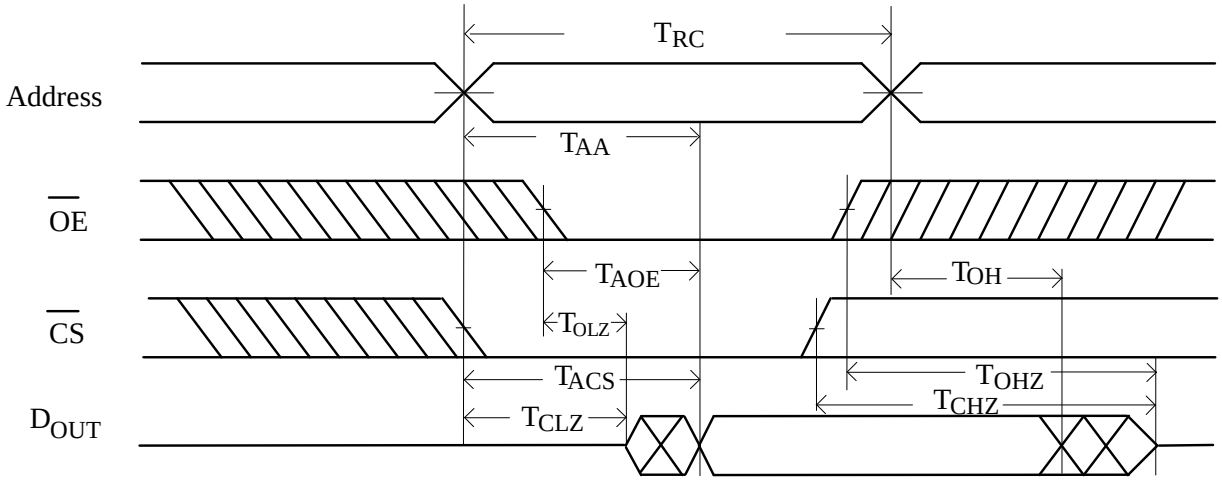
Read Cycle 1 (Address Controlled)



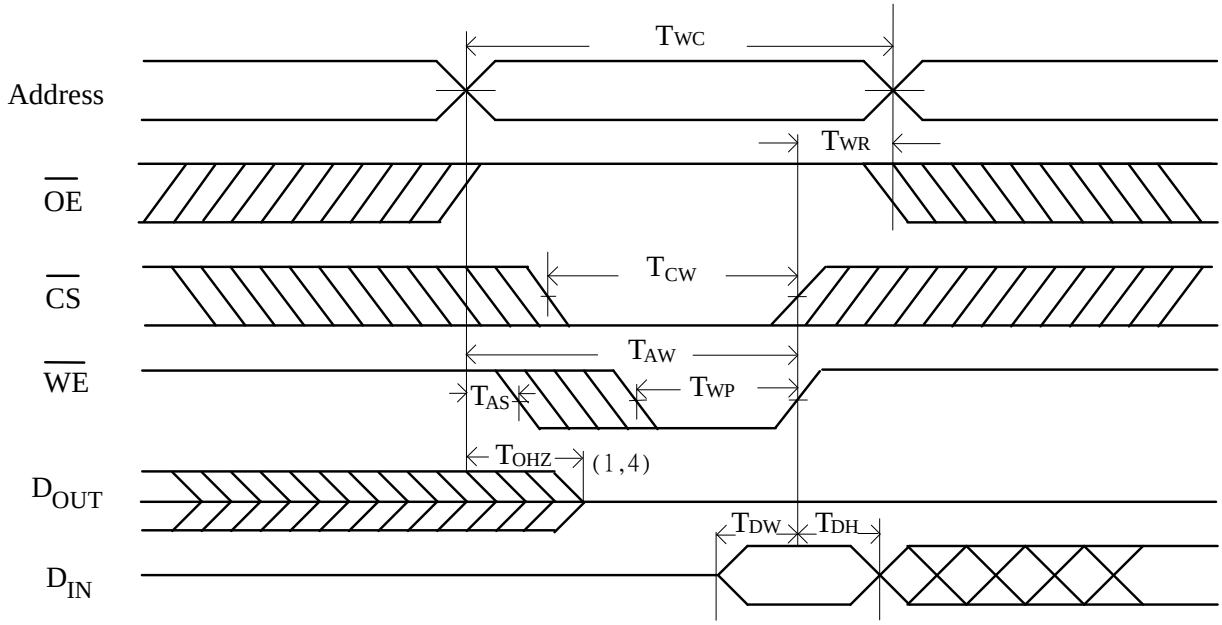
Read Cycle 2 (Chip Select Controlled)



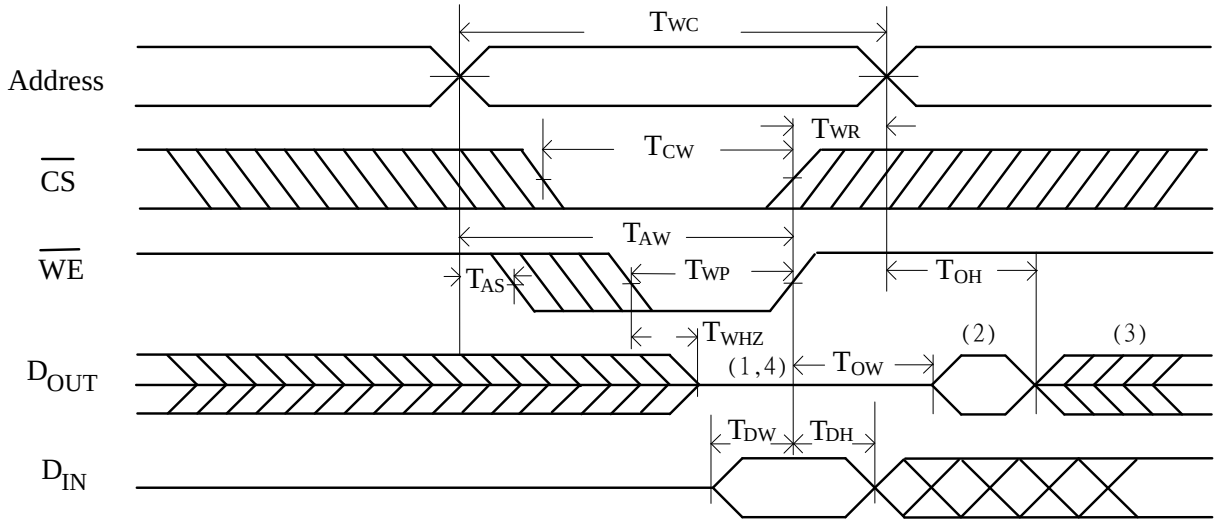
Read Cycle 3 (Output Enable Controlled)



Write Cycle 1 ($\overline{OE}$ Clock)

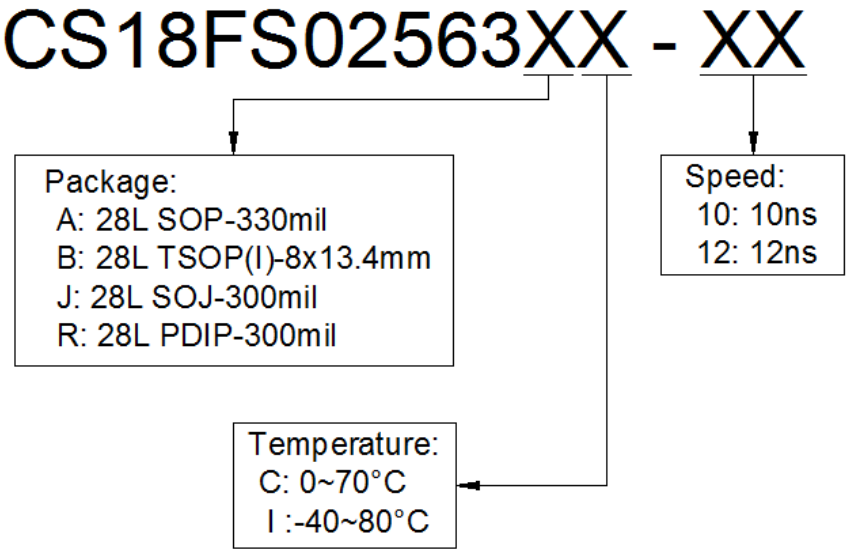


Write Cycle 2 ($\overline{OE}$ = V_{IL} Fixed)



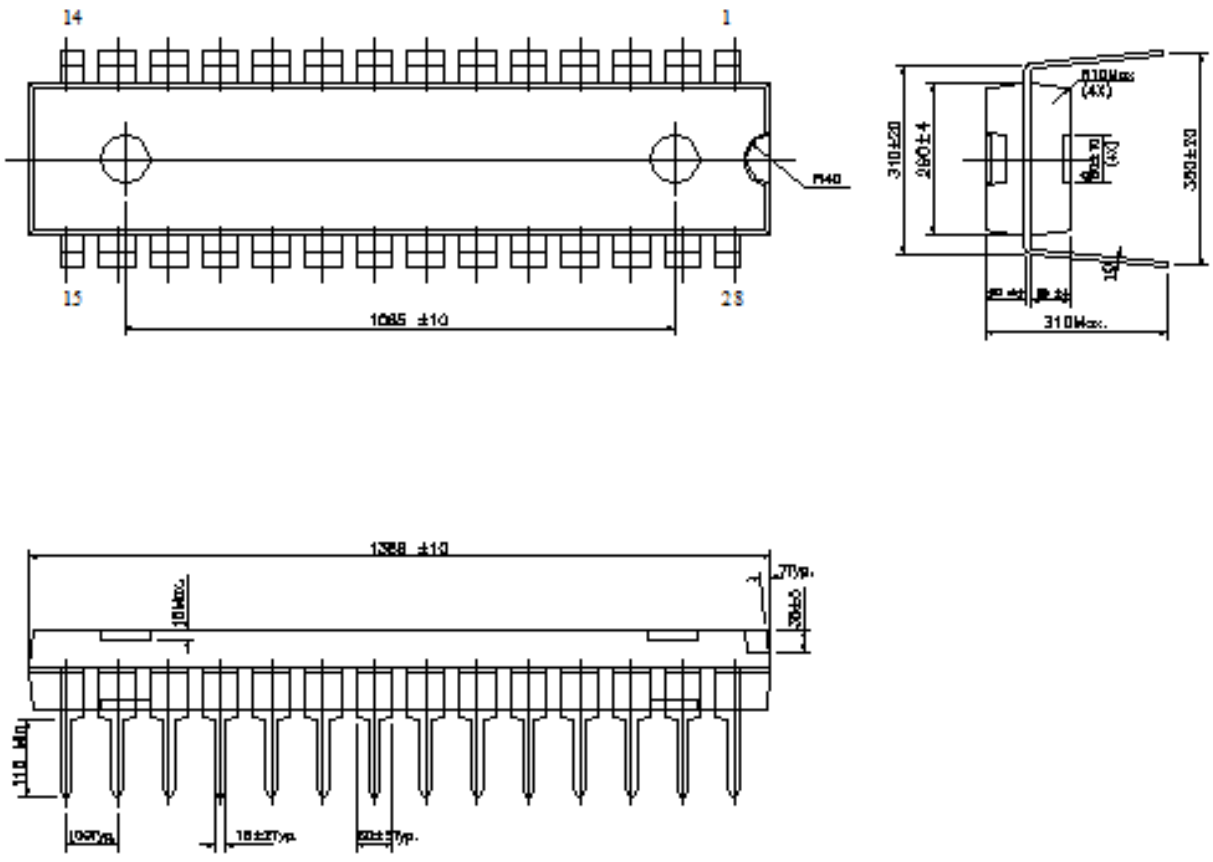
1. *During this period, I/O pins are in the output state, so input signals of opposite phase to the outputs should not be applied.*
2. *The data output from DOUT are the same as the data written to DIN during the write cycle.*
3. *DOUT provides the read data for the next address.*
4. *Transition is measured ±500mV from steady state with CL = 5pF. This parameter is guaranteed but not 100% tested.*

ORDER INFORMATION



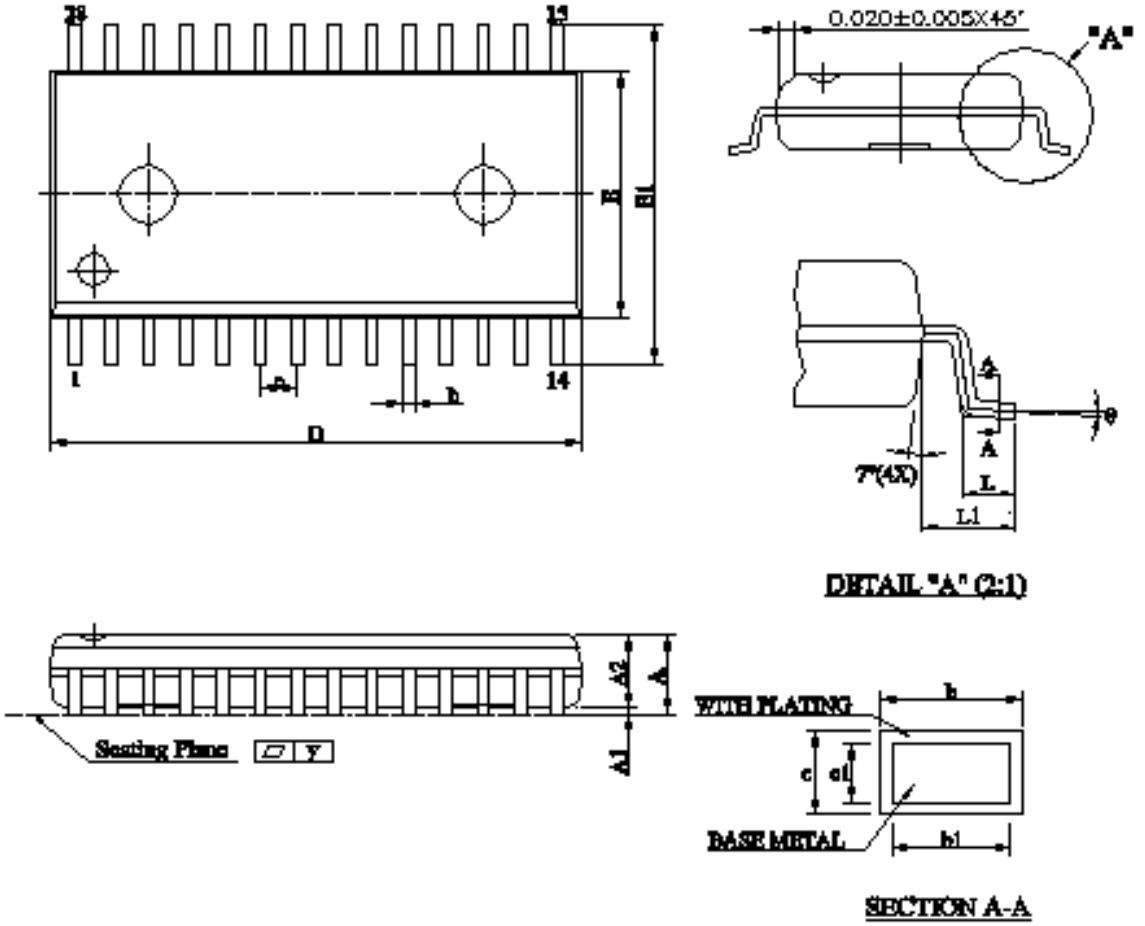
PACKAGE OUTLINE

28 pin PDIP-300mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil

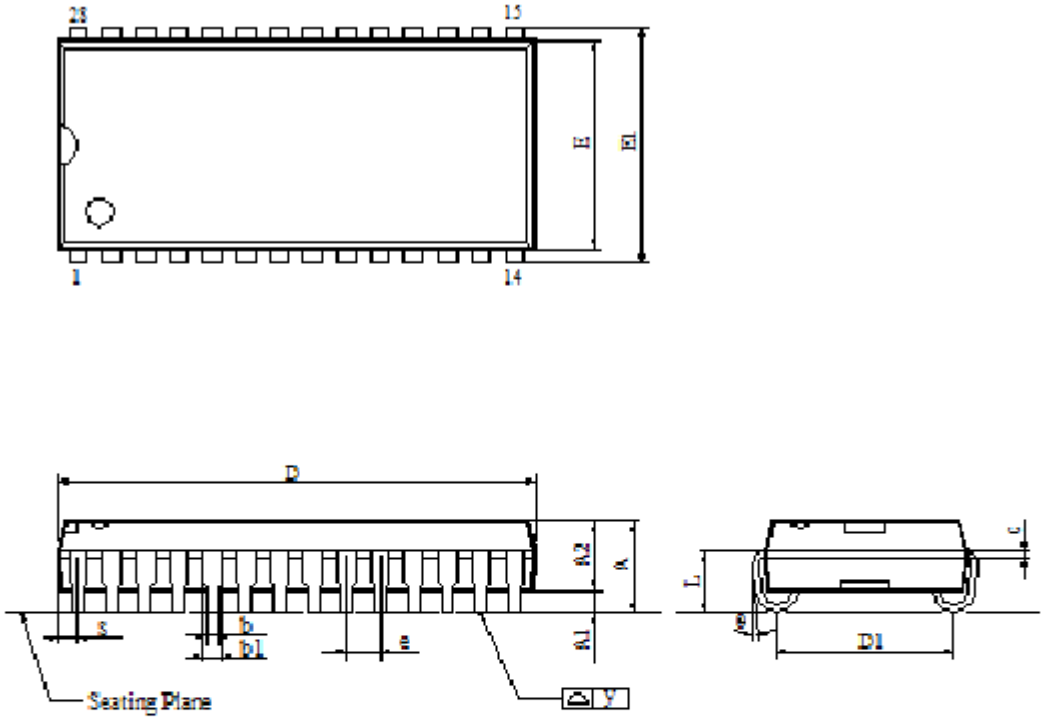
28 pin SOP-330mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	θ
mm	Min.	2.540	0.102	2.362	0.35	0.35	0.20	0.20	17.983	8.280	11.506	1.118	0.700	1.520	–	0°
	Nom.	2.692	0.226	2.489	–	–	–	–	18.110	8.407	11.811	1.270	0.964	1.720	–	–
	Max.	2.844	0.350	2.616	0.50	0.45	0.32	0.28	18.237	8.534	12.116	1.422	1.228	1.920	0.1	10°
inch	Min.	0.100	0.004	0.093	0.014	0.014	0.008	0.008	0.708	0.326	0.453	0.044	0.0276	0.0598	–	0°
	Nom.	0.106	0.009	0.098	–	–	–	–	0.713	0.331	0.465	0.050	0.0380	0.0677	–	–
	Max.	0.112	0.014	0.103	0.020	0.018	0.012	0.011	0.718	0.336	0.477	0.056	0.0484	0.0756	0.004	10°

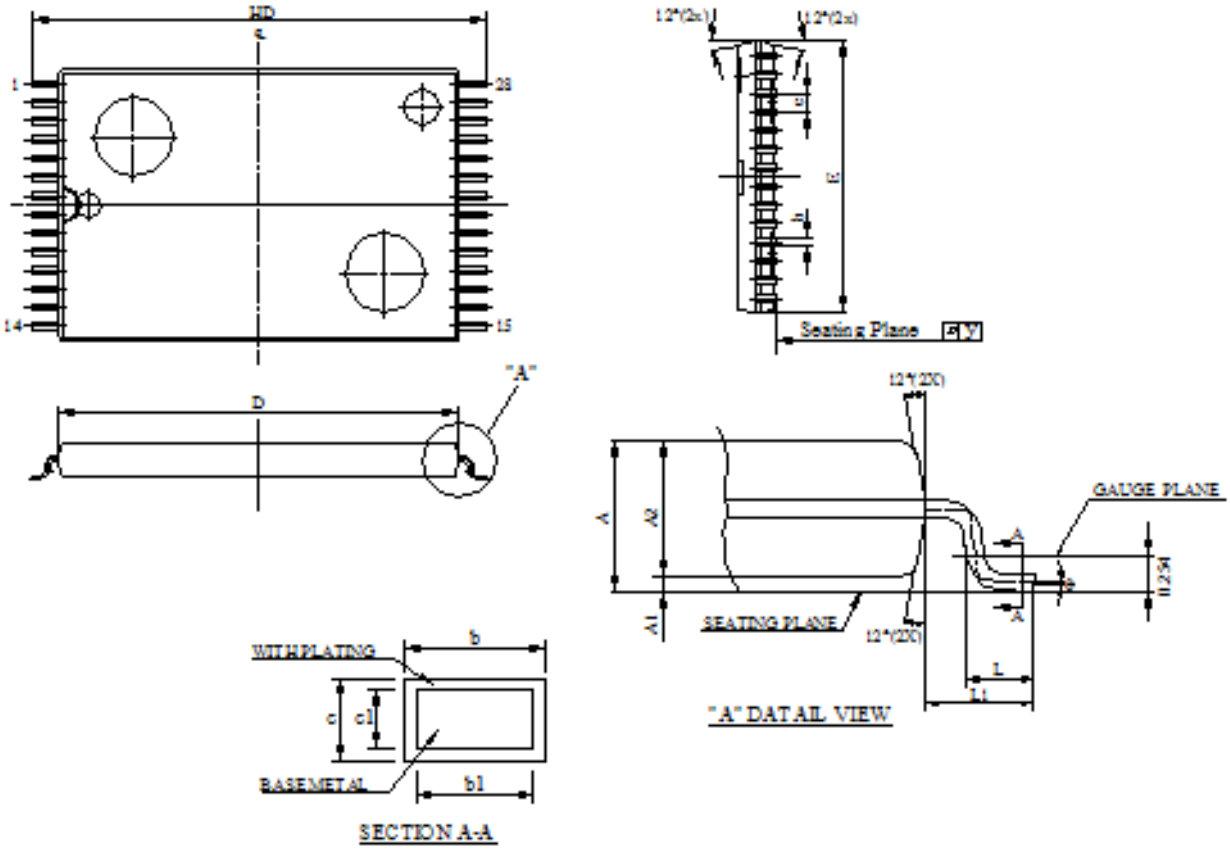
28pin SOJ-300mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL / UNIT		A	A1	A2	b1	b	e	D	E	e	D1	E1	L	S	y	θ
mm	Min.	–	0.69	2.41	0.66	0.41	0.20	–	7.49	1.12	6.22	8.31	1.96	–	–	0°
	Nom.	–	–	2.54	0.71	0.46	0.25	18.03	7.62	1.27	6.73	8.56	2.21	–	–	–
	Max.	3.56	–	2.67	0.81	0.56	0.36	18.54	7.75	1.42	7.24	8.81	2.46	1.14	0.10	10°
inch	Min.	–	0.027	0.095	0.026	0.016	0.008	–	0.295	0.044	0.245	0.327	0.077	–	–	0°
	Nom.	–	–	0.100	0.028	0.018	0.010	0.710	0.300	0.050	0.265	0.337	0.087	–	–	–
	Max.	0.140	–	0.105	0.032	0.022	0.014	0.730	0.305	0.056	0.285	0.347	0.097	0.045	0.004	10°

28 pin TSOP(I)-8x13.4mm



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil

SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	e	HD	L	L1	y	θ
mm	Min.	1.00	0.050	0.95	0.17	0.17	0.10	0.10	11.70	7.90	0.45	13.20	0.40	0.70	–	0°
	Nom.	1.10	0.115	1.00	0.22	0.20	–	–	11.80	8.00	0.55	13.40	0.50	0.80	–	–
	Max.	1.20	0.180	1.05	0.27	0.23	0.21	0.16	11.90	8.10	0.65	13.60	0.70	0.90	0.1	8°
inch	Min.	0.0393	0.0019	0.037	0.007	0.007	0.004	0.004	0.461	0.311	0.018	0.520	0.0157	0.0275	–	0°
	Nom.	0.0433	0.0045	0.039	0.009	0.008	–	–	0.465	0.315	0.022	0.528	0.0197	0.0315	–	–
	Max.	0.0473	0.0071	0.041	0.011	0.009	0.008	0.006	0.469	0.319	0.026	0.536	0.0277	0.0355	0.004	8°