Revision History

Rev. No.	History	Issue Date	Remark
2.0	Initial issue with new naming rule	Jan.18,2005	
2.1	Remove 48TSOP package	Jan.11,2007	
2.2	Revise AC/DC Char.	Mar. 11, 2008	
2.3	Add 48 BGA_6x7mm	Jun. 25, 2008	

GENERAL DESCRIPTION

The CS16LV40963 is a high performance, high speed, super low power CMOS Static Random Access Memory organized as 262,144 words by 16 bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed and low power features with a typical CMOS standby current of 0.50uA and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable (/CE) and active LOW output enable (/OE) and three-state output drivers.

The CS16LV40963 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV40963 is available in JEDEC standard 44-pin TSOP 2 and 48-pin BGA package.

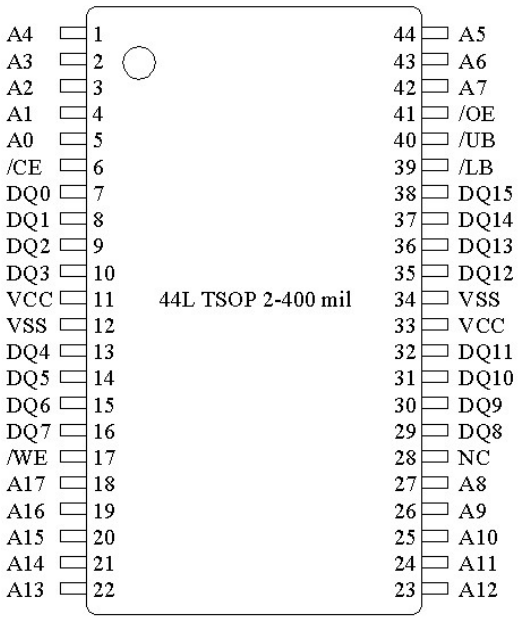
FEATURES

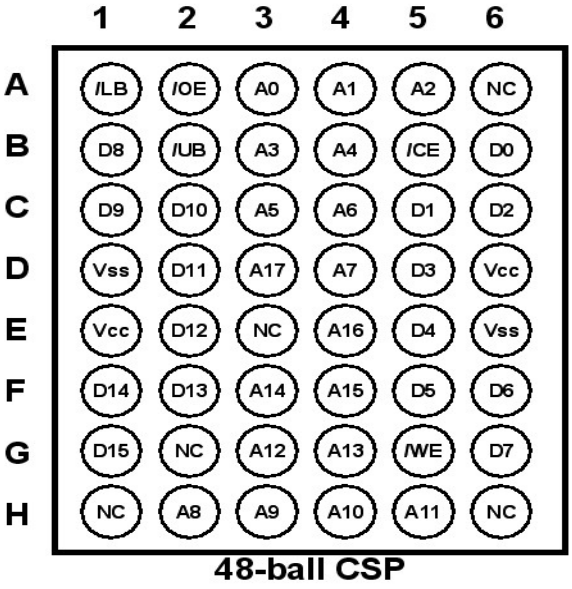
- Low operation voltage : 2.7 ~ 3.6V
- Ultra low power consumption :
  - V_{CC} = 3.0V, 3mA@1MHz (Typ.) operating current
  - 0.5uA (Typ.) CMOS standby current
- High speed access time: 55/70ns (Max.) at V_{CC} = 3.0V.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible, fully static operation
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.

Product Family

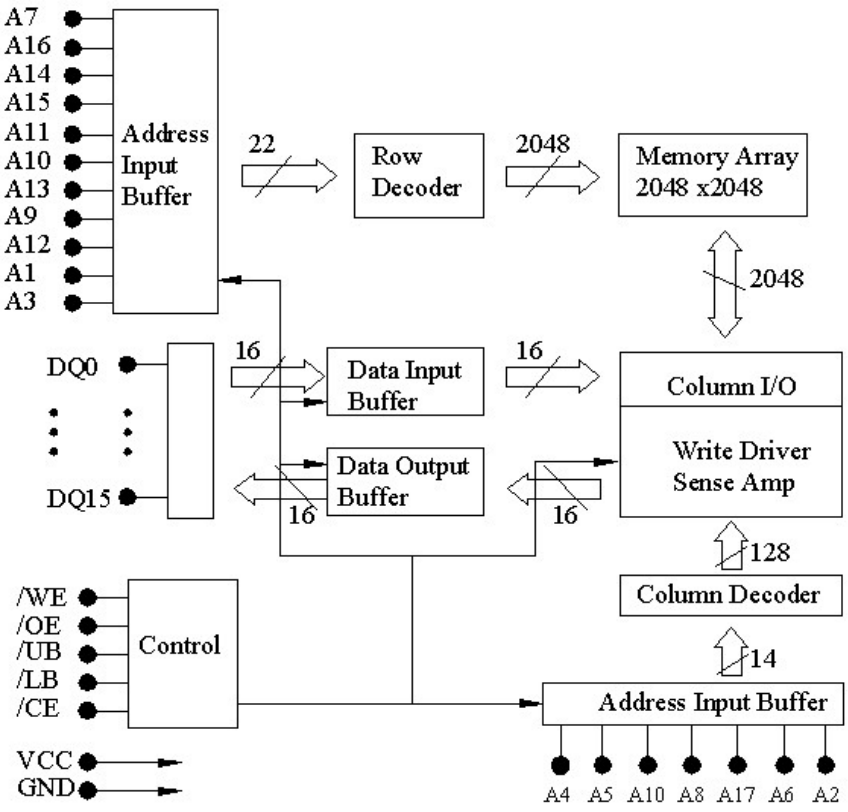
Product Family	Operating Temp	Vcc. Range (V)	Speed (ns)	Standby (Typ.)	Package Type
CS16LV40963	0~70°C	2.7~3.6	55/70	0.5 uA (V_{CC} = 3.0V)	44 TSOP 2-400mil 48 BGA_6x7mm Dice
	-40~85°C		55/70	1.0 uA (V_{CC}= 3.0V)	

PIN CONFIGURATIONS





FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A17	Input	Address inputs for selecting one of the 262,144 x 16 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
Gnd	Power	Ground

TRUTH TABLE

MODE	/CE	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	V_{CC} Current
Standby	X	X	X	H	H	High Z	High Z	I_{CCSB}, I_{CCSB1}
	H	X	X	X	X			
Output Disabled	L	H	H	X	X	High Z	High Z	I_{CC}
Read	L	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
				H	L	High Z	D_{OUT}	I_{CC}
				L	H	D_{OUT}	High Z	I_{CC}
Write	L	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
				H	L	X	D_{IN}	I_{CC}

				L	H	D_{IN}	X	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	30	mA

1. *Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

DC ELECTRICAL CHARACTERISTICS (T_A = 0℃ to 70℃, V_{CC} = 3.0V)

Parameter Name	Parameter	Test Conduction	MIN	TYP (1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage		-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage		2.0		V_{CC}+ 0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE=V_{IN}, or /OE=V_{IN} , V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} = 2mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1mA	2.4			V
		I_{OH} = -100uA	V_{CC} -0.2			
I_{CC}	Operating Power Supply Current	/CE=V_{IL}, I_{DQ}=0mA, F=F_{MAX}(2)			30	mA
I_{CCSB}	Standby Supply - TTL	/CE=V_{IH}, I_{DQ}=0mA,			1	mA
I_{CCSB1}	Standby Current -CMOS	/CE≧V_{CC}-0.2V, V_{IN}≧		0.5	5	uA

		V_{CC}-0.2V or V_{IN}≦0.2V				

1. *Typical characteristics are at T_A = 25℃*

2. *Fmax = 1/t_{RC}.*

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70°C	2.7V ~ 3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

1. *Overshoot : V_{CC} +2.0V in case of pulse width ≦20ns.*

2. *Undershoot : - 2.0V in case of pulse width ≦20ns.*

3. *Overshoot and undershoot are sampled, not 100% tested.*

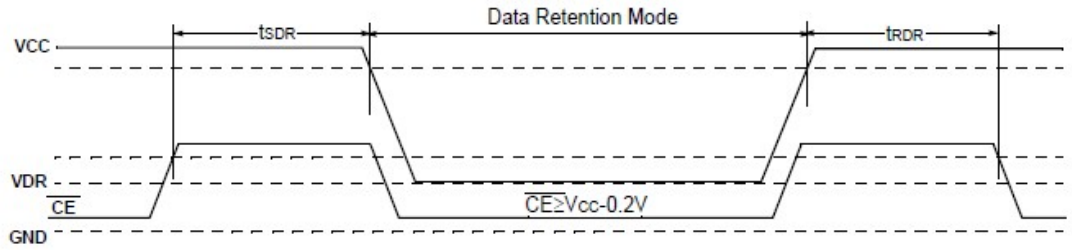
DATA RETENTION CHARACTERISTICS (T_A = 0℃ to + 70℃)

Parameter Name	Parameter	Test Conduction	MIN	TYP (1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE≧V_{CC}-0.2V, V_{CC}=1.5V V_{IN}≧ V_{CC}-0.2V or V_{IN}≦0.2V		0.3	2	uA
T_{CDR}	Chip Deselect to Data Retention Time	See Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

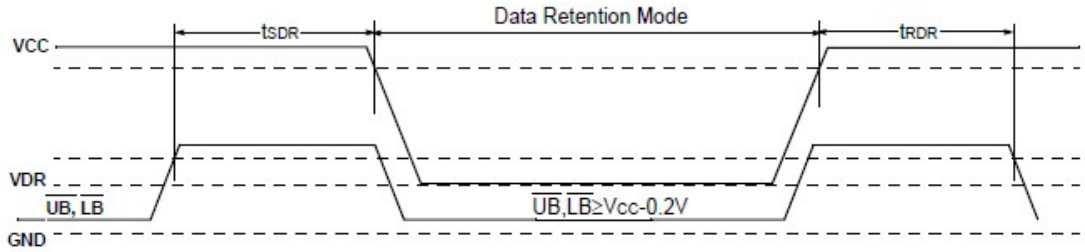
1. *V_{CC}= 3.0V, T_A = + 25℃*

2. *t_{RC} (2) = Read Cycle Time.*

LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (/UB, /LB Controlled)



CAPACITANCE (1) (TA = 25°C, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/Output Capacitance	$V_{I/O}$=0V	8	pF

This parameter is guaranteed and not tested.

AC TEST CONDITIONS

Input Pulse Levels	Vcc/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	See FIGURE 1A and 1B

KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

AC TEST LOADS AND WAVEFORMS

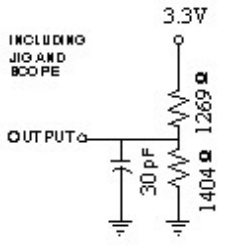


FIGURE 1A

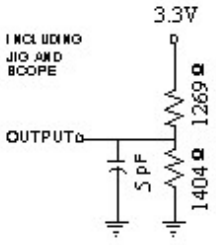


FIGURE 1B

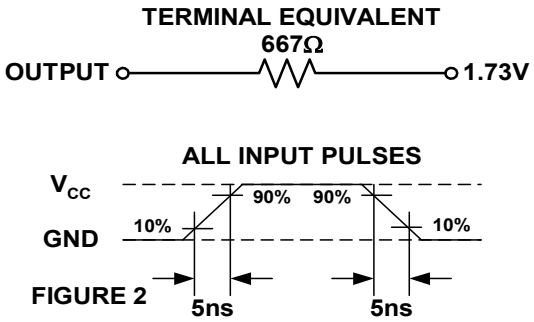


FIGURE 2

AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ to + 70℃, V_{CC} = 3V)

< READ CYCLE >

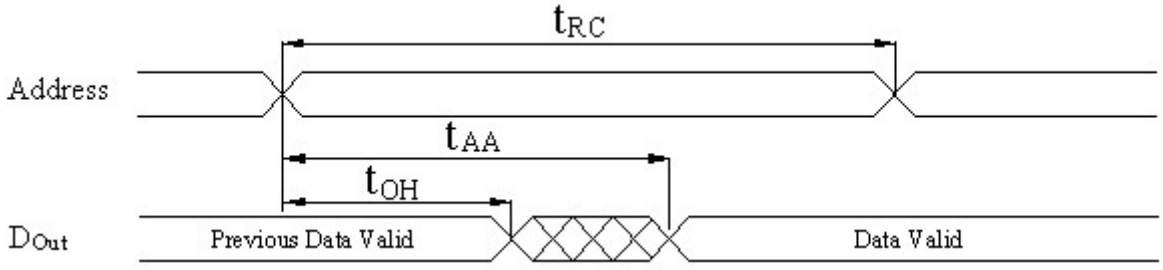
JEDEC Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{ACS}	Chip Select Access Time (/CE)		55		70	ns
t_{BA}	t_{BA}	Data Byte Control Access Time (/LB, /UB)		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		25		35	ns
t_{ELQX}	t_{CLZ}	Chip Select to Output Low Z (/CE)	10		10		ns
t_{BE}	t_{BE}	Data Byte Control to Output Low Z (/LB, /UB)	5		5		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{CHZ}	Chip Deselect to Output in High Z (/CE)	0	20	0	25	ns
t_{BDO}	t_{BDO}	Data Byte Control to Output High Z (/LB, /UB)	0	20	0	25	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	0	25	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		ns

NOTES:

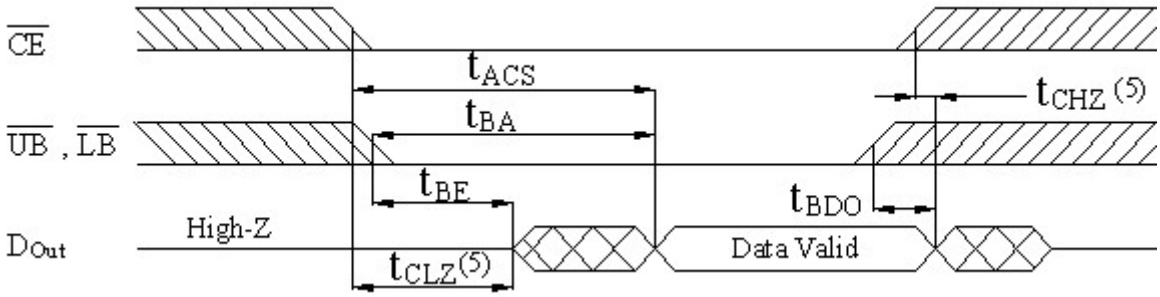
1. */WE is high in read Cycle.*
2. *Device is continuously selected when /CE = V_{IL}.*
3. *Address valid prior to or coincident with CE transition low.*
4. */OE = V_{IL}.*
5. *Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.*

SWITCHING WAVEFORMS (READ CYCLE)

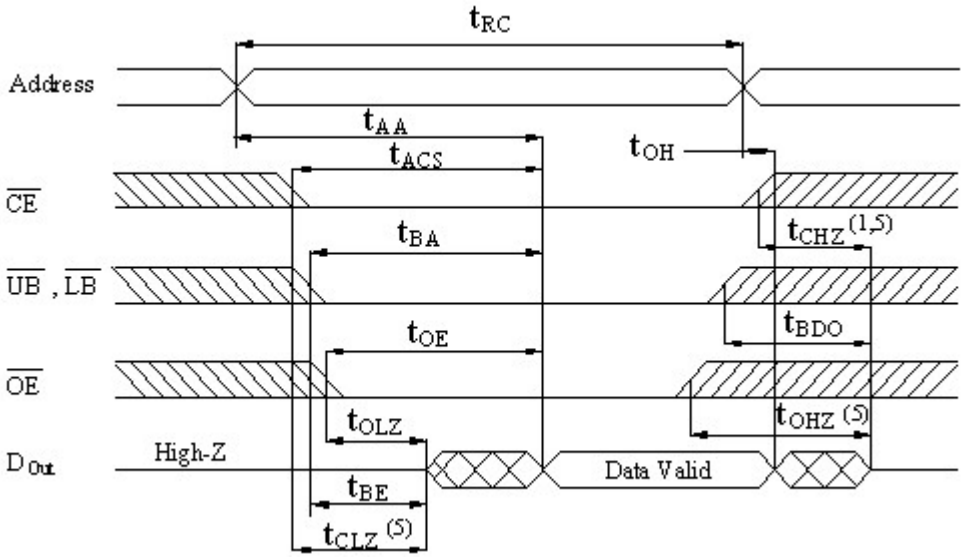
READ CYCLE 1. (1, 2, 4)



READ CYCLE 2. (1, 3, 4)



READ CYCLE 3. (1, 4)



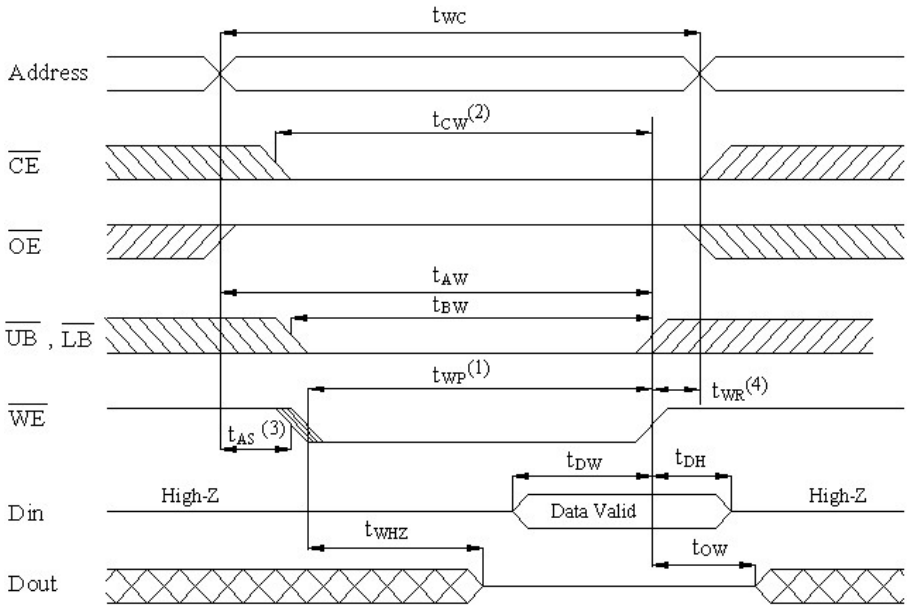
AC ELECTRICAL CHARACTERISTICS (T_A = 0 ℃to + 70℃, V_{CC} = 3V)

< WRITE CYCLE >

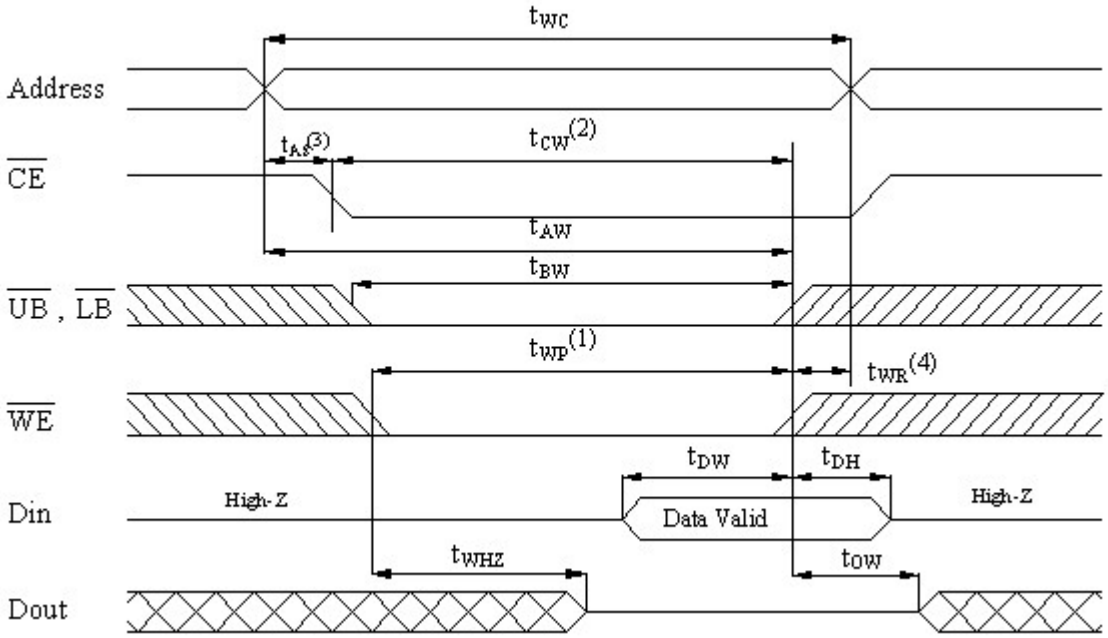
JEDEC Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR1}	Write Recovery Time (/CE, /WE)	0		0		ns
t_{BW}	t_{BW}	Data Byte Control to End of Write(/LB, /UB)	45		60		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		25		30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold from Write Time	0		0		ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

■ SWITCHING WAVEFORMS (WRITE CYCLE)

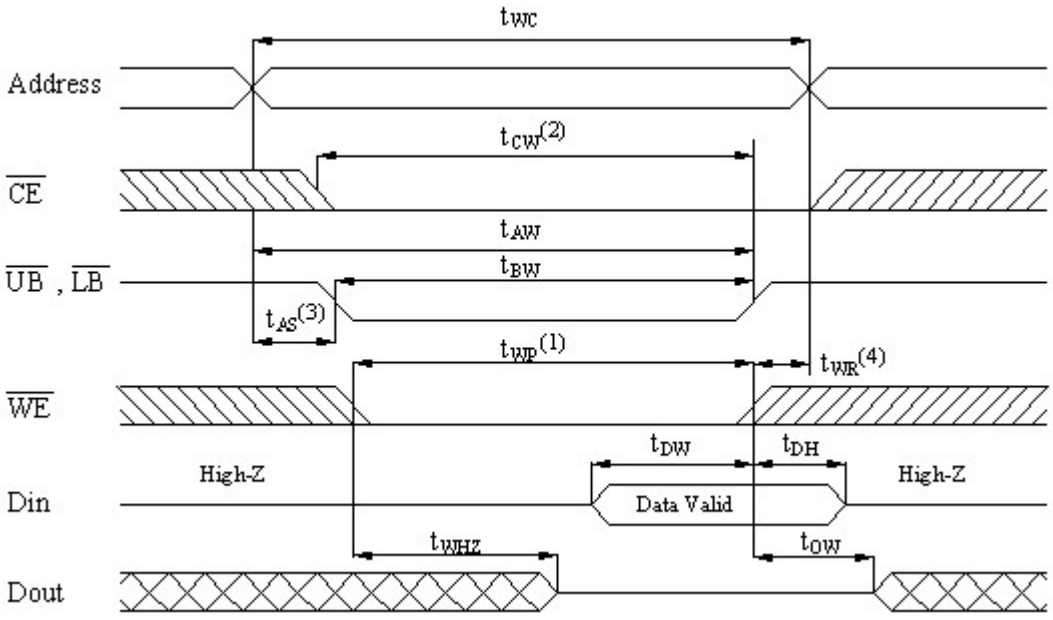
WRITE CYCLE 1. (/WE Controlled)



WRITE CYCLE 2. (/CE1 and CE2 Controlled)



WRITE CYCLE 3. (/UB and /LB Controlled)

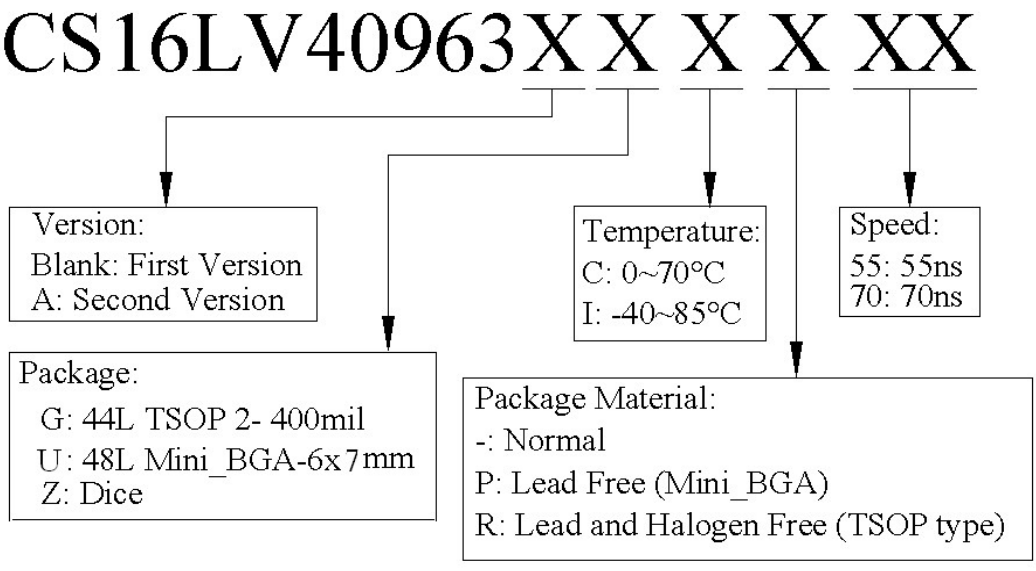


NOTES:

1. *T_{AS} is measured from the address valid to the beginning of write.*

2. *The internal write time of the memory is defined by the overlap of /CE and /WE low. All signals must be active to initiate a write and any one signal can terminate a write by going inactive. The data input setup and hold timing should be referenced to the second transition edge of the signal that terminates the write.*
3. *TWR is measured from the earliest of /CE or /WE or (/UB and ,or /LB) going high at the end of write cycle.*
4. *During this period, DQ pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.*
5. *If the /CE low transition occurs simultaneously with the /WE low transitions or after the /WE transition, output remain in a high impedance state.*
6. */OE is continuously low (/OE = VIL).*
7. *DOUT is the same phase of write data of this write cycle.*
8. *DOUT is the read data of next address.*
9. *If /CE is low during this period, DQ pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.*
10. *Transition is measured ±500mV from steady state with CL = 5pF as shown in Figure 1B. The parameter is guaranteed but not 100% tested.*
11. *TCW is measured from the later of /CE going low to the end of write.*

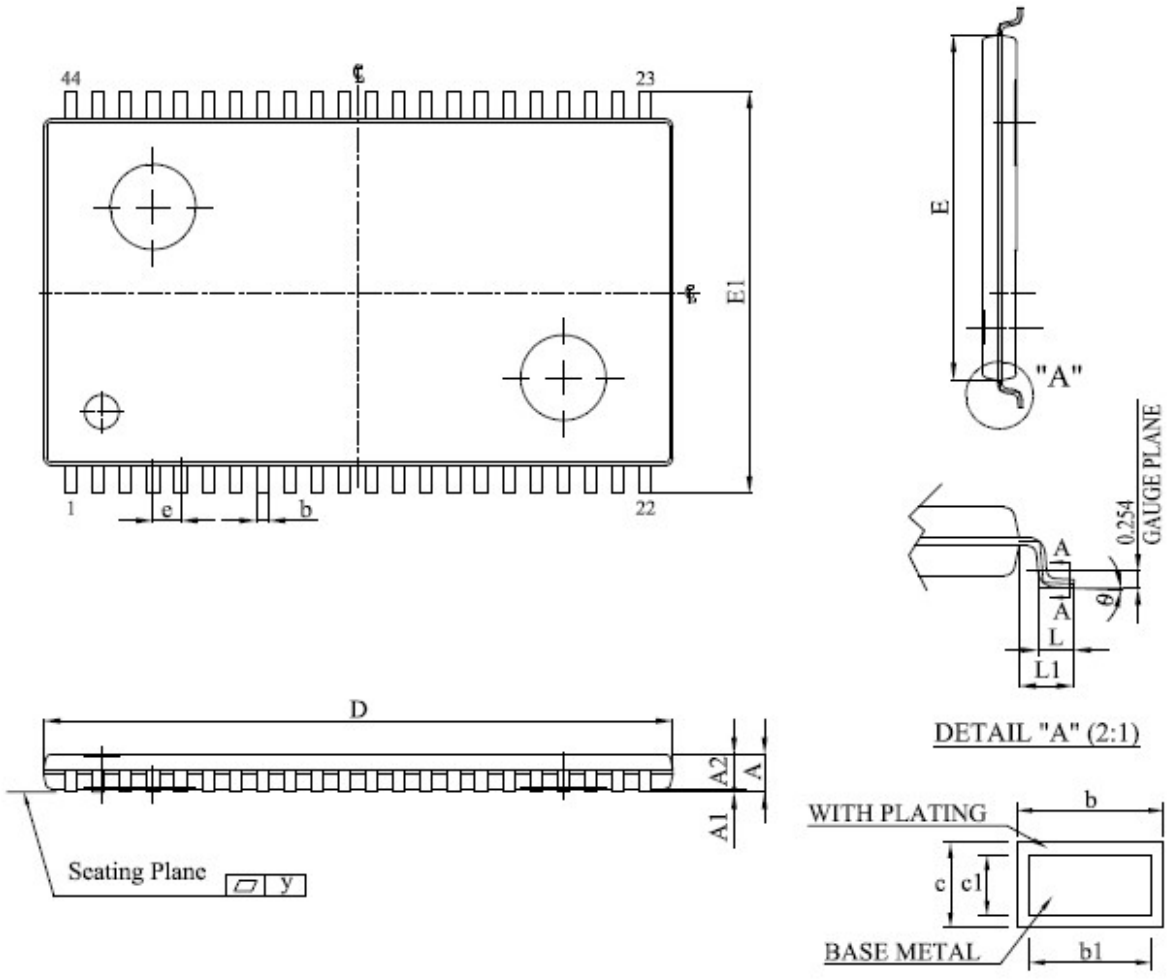
ORDER INFORMATION



Note: Package material code "P" & "R" meets ROHS.

PACKAGE OUTLINE

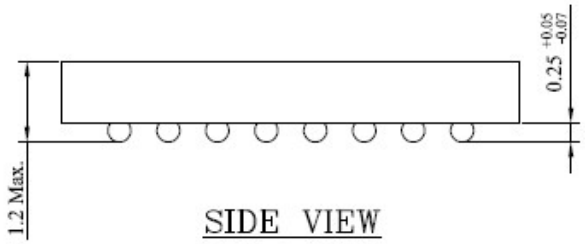
44L TSOP2-400MIL



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

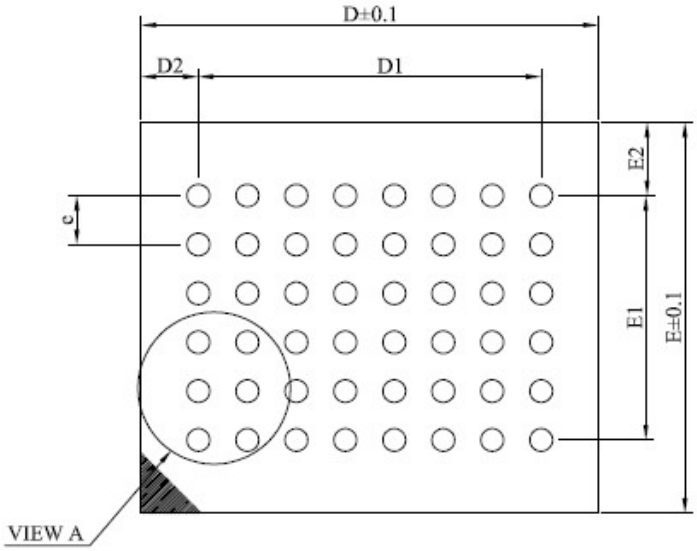
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

48 ball Mini BGA-6x7mm

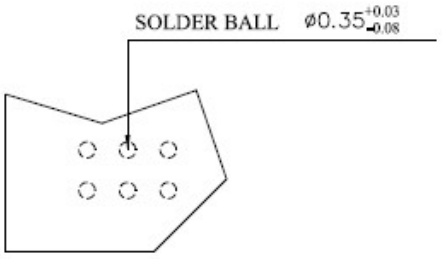


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
7.0	6.0	48	5.25	3.75	0.875	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025