Revision History

Rev. No.	History	Issue Date	Remark
1.0	Initial issue	Jan.17, 2005	
1.1	Add 48 CSP-6x8mm	Sep. 16, 2005	
1.2	Revise DC characteristics	Apr. 11, 2008	
1.3	Remove 48 Mini BGA 6*8 mm package type Add 48 Mini BGA 6*7 mm package type	Jul. 05, 2010	

GENERAL DESCRIPTION

The CS16LV20493 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 131,072 words by 16bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable inputs (/CE1, CE2) and active LOW output enable (/OE).
The CS16LV20493 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV20493 is available in JEDEC standard 44-pin TSOP 2 and 48-ball mini_BGA-6x7mm packages.

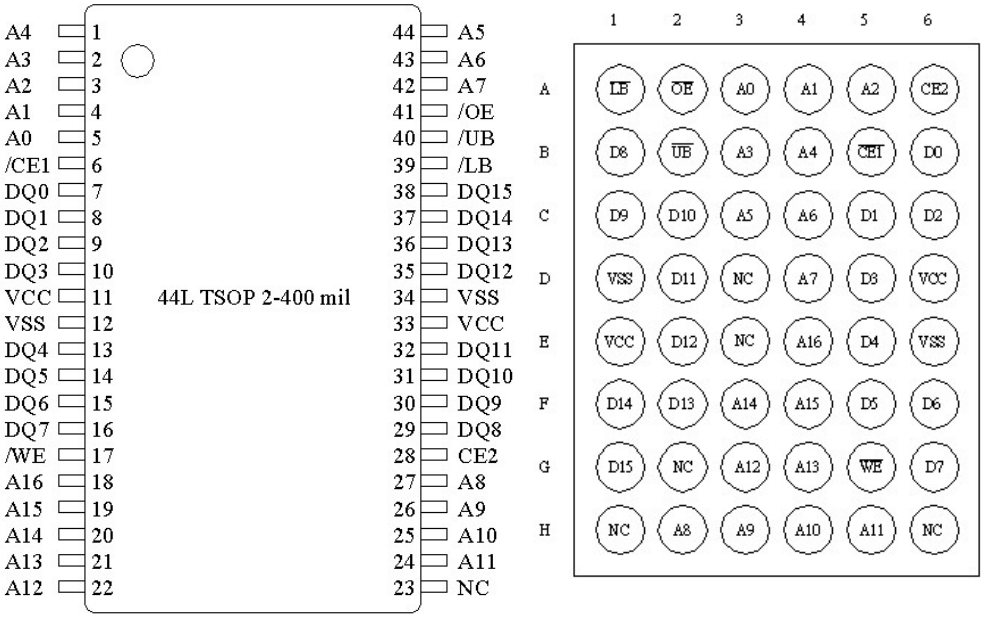
FEATURES

- Wide operation voltage : 2.7 ~ 3.6V
- Ultra-low power consumption :
  - 3mA@1MHz (Max.), Vcc=3.0V.
  - 0.5 uA (Typ.) CMOS standby current
- High speed access time: 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with (/CE1, CE2) and /OE options.

Product Family

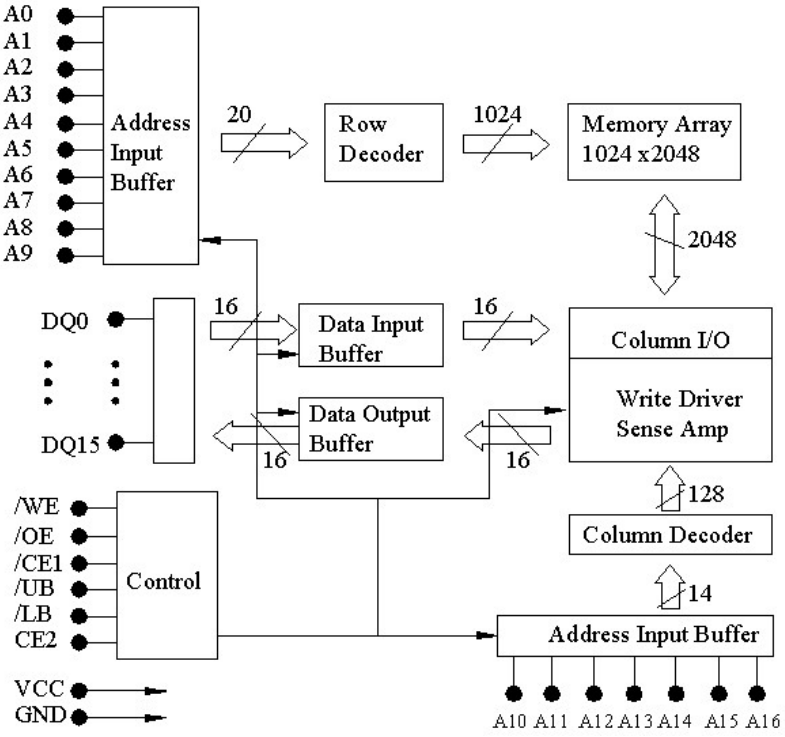
Part No.	Operating Temp	V_{CC}. Range	Speed (ns)	Standby (Typ.)	Package Type
CS16LV20493	0~70°C	2.7~3.6	55/ 70	0.5uA (V_{CC} = 3.0V)	44 TSOP 2 48 Mini BGA Dice
	-40~85°C		55/ 70	0.8uA (V_{CC}= 3.0V)	

PIN CONFIGURATION



48 ball Mini_BGA-6x7mm Top View

FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

Name	Type	Function
A0 – A16	Input	Address inputs for selecting one of the 131,072 x 16 bit words in the RAM
/CE1, CE2	Input	/CE1 is active LOW and CE2 is active HIGH. Both chip enables must be active when data read from or write to the device. If either chip enable is not active, the device is deselected and in a standby power down mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB, /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V_{CC}	Power	Power Supply
Gnd	Power	Ground

TRUTH TABLE

MODE	/CE1	CE2	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	V_{CC} Current
Standby	X	L	X	X	X	X	High Z	High Z	I_{CCSB}, I_{CCSB1}
	H	X	X	X	X	X			
Output Disabled	L	H	H	H	X	X	High Z	High Z	I_{CC}
			X	X	H	H			
Read	L	H	H	L	L	L	D_{OUT}	D_{OUT}	I_{CC}
					H	L	High Z	D_{OUT}	I_{CC}
					L	H	D_{OUT}	High Z	I_{CC}
Write	L	H	L	X	L	L	D_{IN}	D_{IN}	I_{CC}
					H	L	X	D_{IN}	I_{CC}
					L	H	D_{IN}	X	I_{CC}

ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
V_{TERM}	Terminal Voltage with Respect to GND	-0.5 to Vcc+0.5	V
T_{BIAS}	Temperature Under Bias	-40 to +125	^{O}C
T_{STG}	Storage Temperature	-60 to +150	^{O}C
P_T	Power Dissipation	1.0	W
I_{OUT}	DC Output Current	25	mA

1. *Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.*

OPERATING RANGE

Range	Ambient Temperature	Vcc
Commercial	0~70^{o}C	2.7V ~3.6V
Industrial	-40~85^{o}C	2.7V ~ 3.6V

1. Overshoot : V_{CC} +2.0V in case of pulse width ≤20ns.

2. Undershoot : - 2.0V in case of pulse width ≤20ns.

3. Overshoot and undershoot are sampled, not 100% tested.

CAPACITANCE (1) (T_A = 25℃, f =1.0 MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C_{IN}	Input Capacitance	V_{IN}=0V	6	pF
C_{DQ}	Input/output Capacitance	$V_{I/O}$=0V	8	pF

This parameter is guaranteed, and not 100% tested.

DC ELECTRICAL CHARACTERISTICS (T_A = 0℃~70℃, V_{CC} = 3.0V)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{IL}	Guaranteed Input Low Voltage (2)	V_{CC}=3.0V	-0.5		0.8	V
V_{IH}	Guaranteed Input High Voltage (2)	V_{CC}=3.0V	2.0		Vcc+0.2	V
I_{IL}	Input Leakage Current	V_{CC}=MAX, V_{IN}=0 to V_{CC}	-1		1	uA
I_{OL}	Output Leakage Current	V_{CC}=MAX, /CE1=V_{Ih}, or /OE=V_{Ih} ,or /WE= V_{IL} V_{IO}=0V to V_{CC}	-1		1	uA
V_{OL}	Output Low Voltage	V_{CC}=MAX, I_{OL} =2.0mA			0.4	V
V_{OH}	Output High Voltage	V_{CC}=MIN, I_{OH} = -1.0mA	2.4			V
I_{CC}	Operating Power Supply Current	/CE1=V_{IL}, I_{DQ}=0mA, F=F_{MAX} =1/ t_{RC}			25	mA
I_{CCSB}	TTL Standby Supply	/CE1=V_{IH}, I_{DQ}=0mA,			1	mA
I_{CCSB1}	CMOS Standby Current	/CE1≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V,		0.5	4	uA

1. *Typical characteristics are at T_A = 25℃.*
2. *These are absolute values with respect to device ground and all overshoots due to system or tester notice are included.*
3. *Fmax = 1/t_{RC}.*

DATA RETENTION CHARACTERISTICS (T_A = 0℃ ~70℃)

Name	Parameter	Test Condition	MIN	TYP(1)	MAX	Unit
V_{DR}	V_{CC} for Data Retention	/CE1≧V_{CC}-0.2V, V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V	1.5			V
I_{CCDR}	Data Retention Current	/CE1≧V_{CC}-0.2V, V_{CC} =1.5V V_{IN}≧V_{CC}-0.2V or V_{IN}≦0.2V		0.3	2	uA
T_{CDR}	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
t_R	Operation Recovery Time		t_{RC} (2)			ns

1. T_A = 25℃, 2. t_{RC}= Read Cycle Time

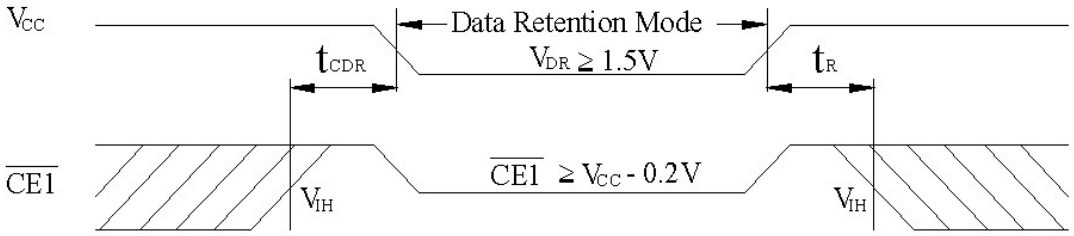
AC TEST CONDITIONS

Input Pulse Levels	V_{CC}/0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5Vcc
Output Load	See FIGURE 1A and 1B

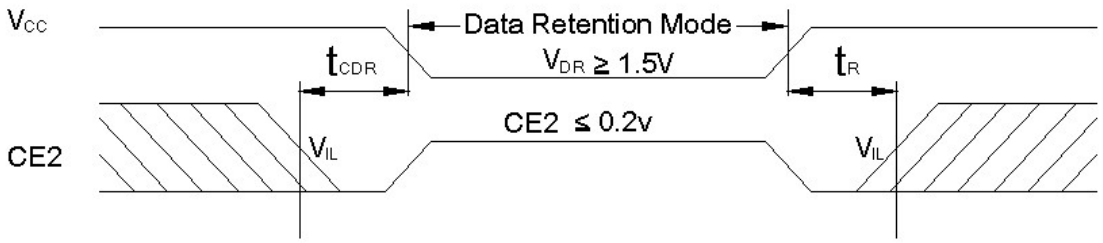
KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

LOW V_{CC} DATA RETENTION WAVEFORM (1) (/CE1 Controlled)



LOW V_{CC} DATA RETENTION WAVEFORM (2) (CE2 Controlled)



AC TEST LOADS AND WAVEFORMS

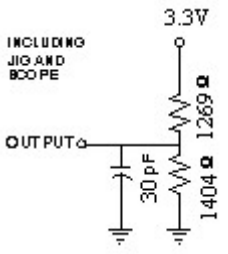


FIGURE 1A

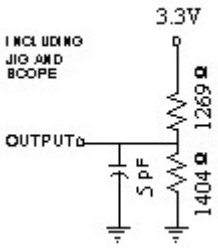
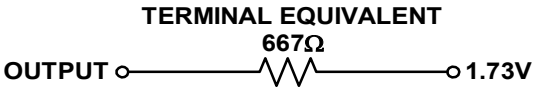


FIGURE 1B



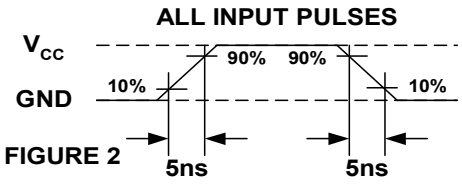


FIGURE 2

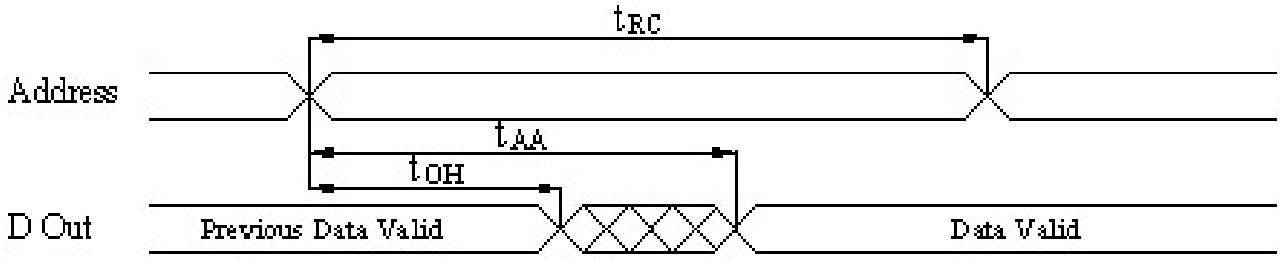
AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃ ; V_{CC}=3.0V)

< READ CYCLE >

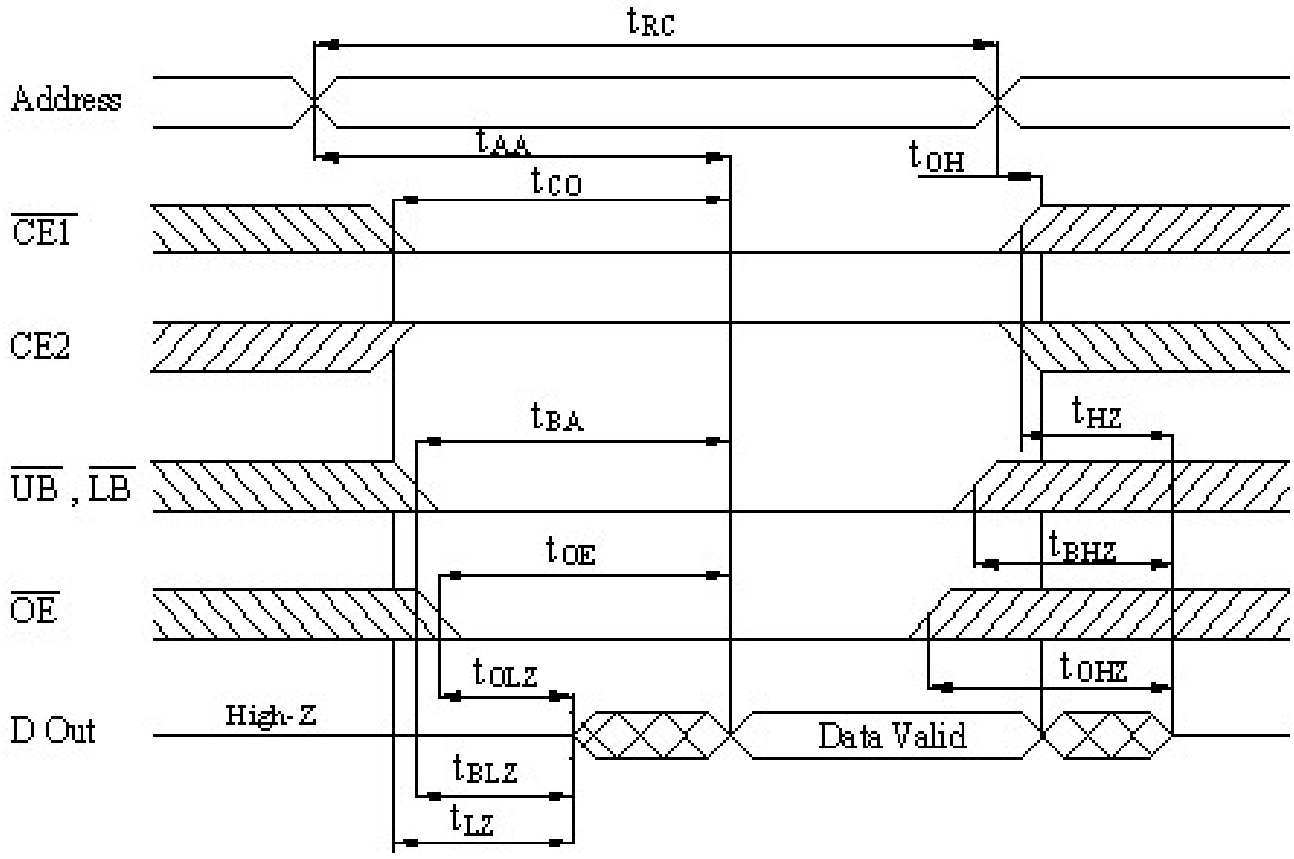
JEDEC Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{RC}	Read Cycle Time	55		70		ns
t_{AVQV}	t_{AA}	Address Access Time		55		70	ns
t_{ELQV}	t_{CO}	Chip Select Access Time (/CE1)		55		70	ns
t_{BA}	t_{BA}	Data Byte Control Access Time (/LB, /UB)		55		70	ns
t_{GLQV}	t_{OE}	Output Enable to Output Valid		25		35	ns
t_{ELQX}	t_{LZ}	ChiChip Select to Output Low Z (/CE1)	10		10		ns
t_{BE}	t_{BLZ}	Data Byte Control to Output Low Z (/LB, /UB)	5		5		ns
t_{GLQX}	t_{OLZ}	Output Enable to Output in Low Z	5		5		ns
t_{EHQZ}	t_{HZ}	Chip Deselect to Output in High Z (/CE1)	0	20	0	25	ns
t_{BDO}	t_{BHZ}	Data Byte Control to Output High Z (/LB, /UB)	0	20	0	25	ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	20	0	25	ns
t_{AXOX}	t_{OH}	Out Disable to Address Change	10		10		ns

SWITCHING WAVEFORMS (READ CYCLE)

READ CYCLE1



READ CYCLE2



NOTES:

1. *t_{HZ} and t_{OHZ} are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.*
2. *At any given temperature and voltage condition, t_{HZ}(Max.) is less than t_{LZ}(Min.) both for a given device and from device to device interconnection.*

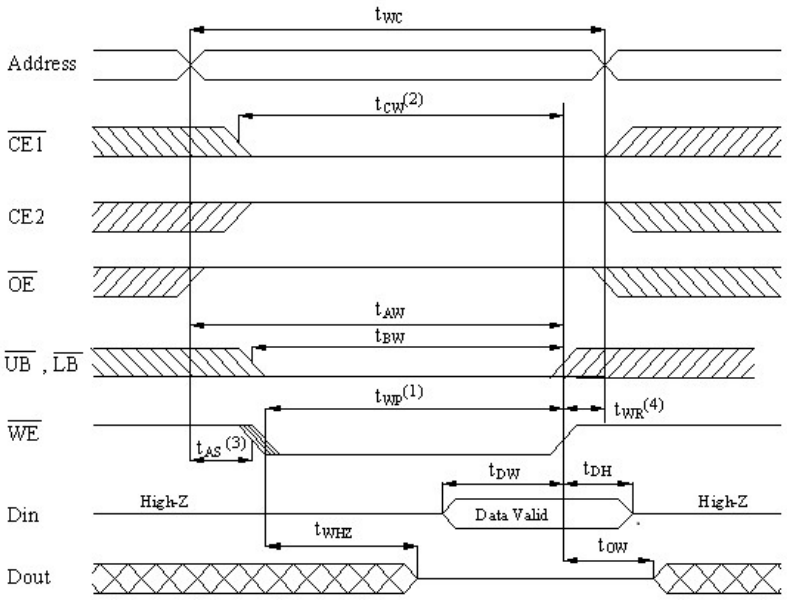
AC ELECTRICAL CHARACTERISTICS (T_A = 0℃ ~70℃ ; V_{CC} = 3.0V)

< WRITE CYCLE >

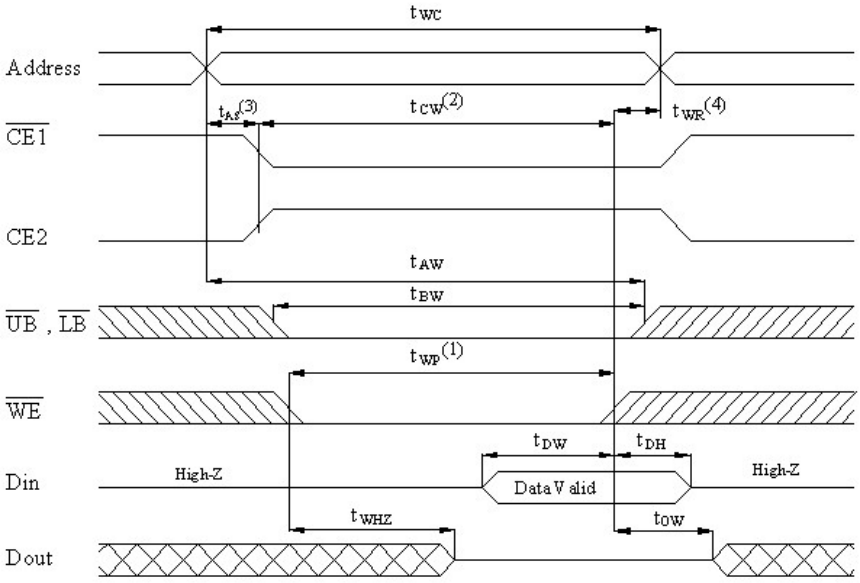
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
t_{AVAX}	t_{WC}	Write Cycle Time	55		70		ns
t_{E1LWH}	t_{CW}	Chip Select to End of Write	45		60		ns
t_{AVWL}	t_{AS}	Address Setup Time	0		0		ns
t_{AVWH}	t_{AW}	Address Valid to End of Write	45		60		ns
t_{BW}	t_{BW}	/UB, /LB valid to end of write	45		60		ns
t_{WLWH}	t_{WP}	Write Pulse Width	40		50		ns
t_{WHAX}	t_{WR}	Write Recovery Time	0		0		ns
t_{WLQZ}	t_{WHZ}	Write to Output in High Z		25		30	ns
t_{DVWH}	t_{DW}	Data to Write Time Overlap	25		30		ns
t_{WHDX}	t_{DH}	Data Hold for Write End	0		0		ns
t_{GHQZ}	t_{OHZ}	Output Disable to Output in High Z	0	30	0	30	ns
t_{WHOX}	t_{OW}	End of Write to Output Active	5		5		ns

SWITCHING WAVEFORMS (WRITE CYCLE)

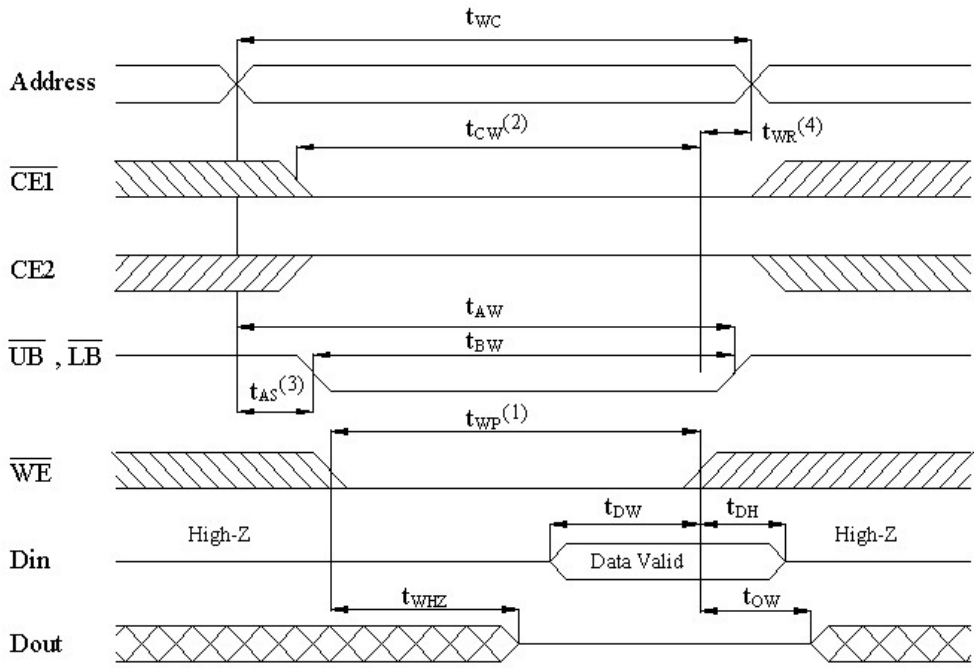
WRITE CYCLE 1. (/WE CONTROLLED)



WRIRE CYCLE 2. (/CE1 AND CE2 CONTROLLED)



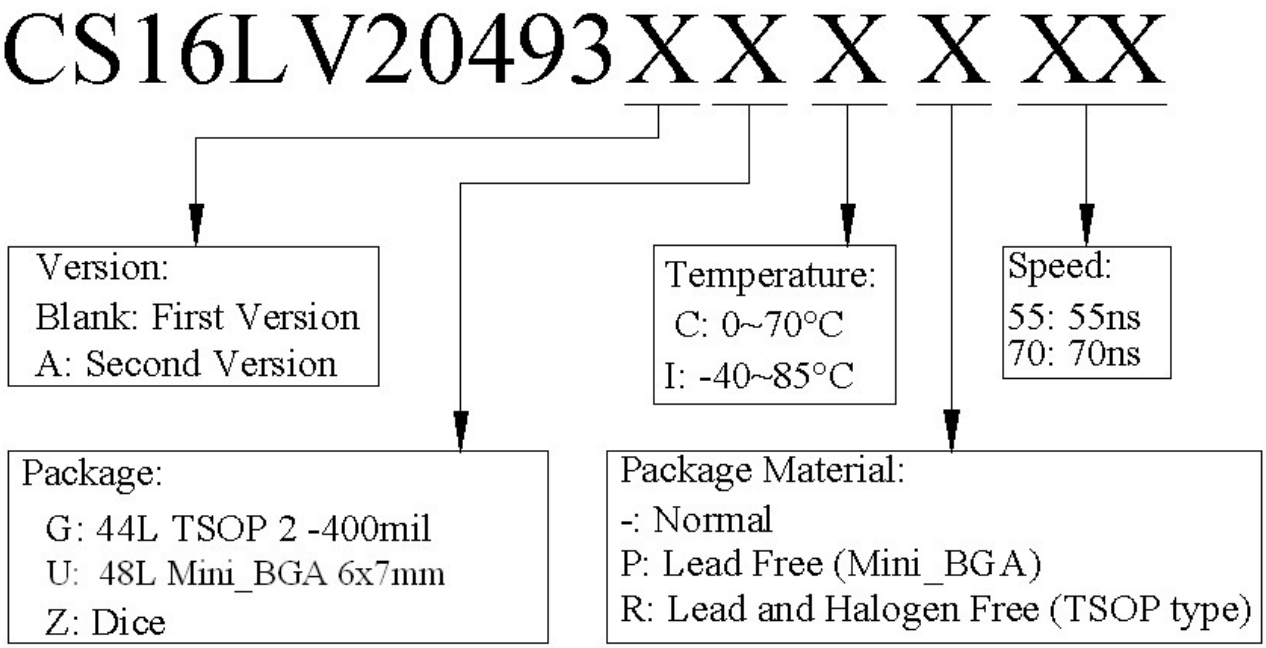
WRIRE CYCLE 3. (/UB AND /LB CONTROLLED)



NOTES:

1. *A write occurs during the overlap(tWP) of low /CE1, high CE2 and low /WE. A write begins when /CE1 goes low and /WE goes low with asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CE1 goes high, CE2 goes low and /WE goes high. The t_{WP} is measured from the beginning of the write to the end of write.*
2. *t_{CW} is measured from the /CE1 going low or CE2 going low to end of write.*
3. *t_{AS} is measured from the address valid to the beginning of write.*
4. *t_{WR} is measured from the end or write to the address change. TWR applied in case a write ends as /CE1 or /WE going high or CE2 going low.*

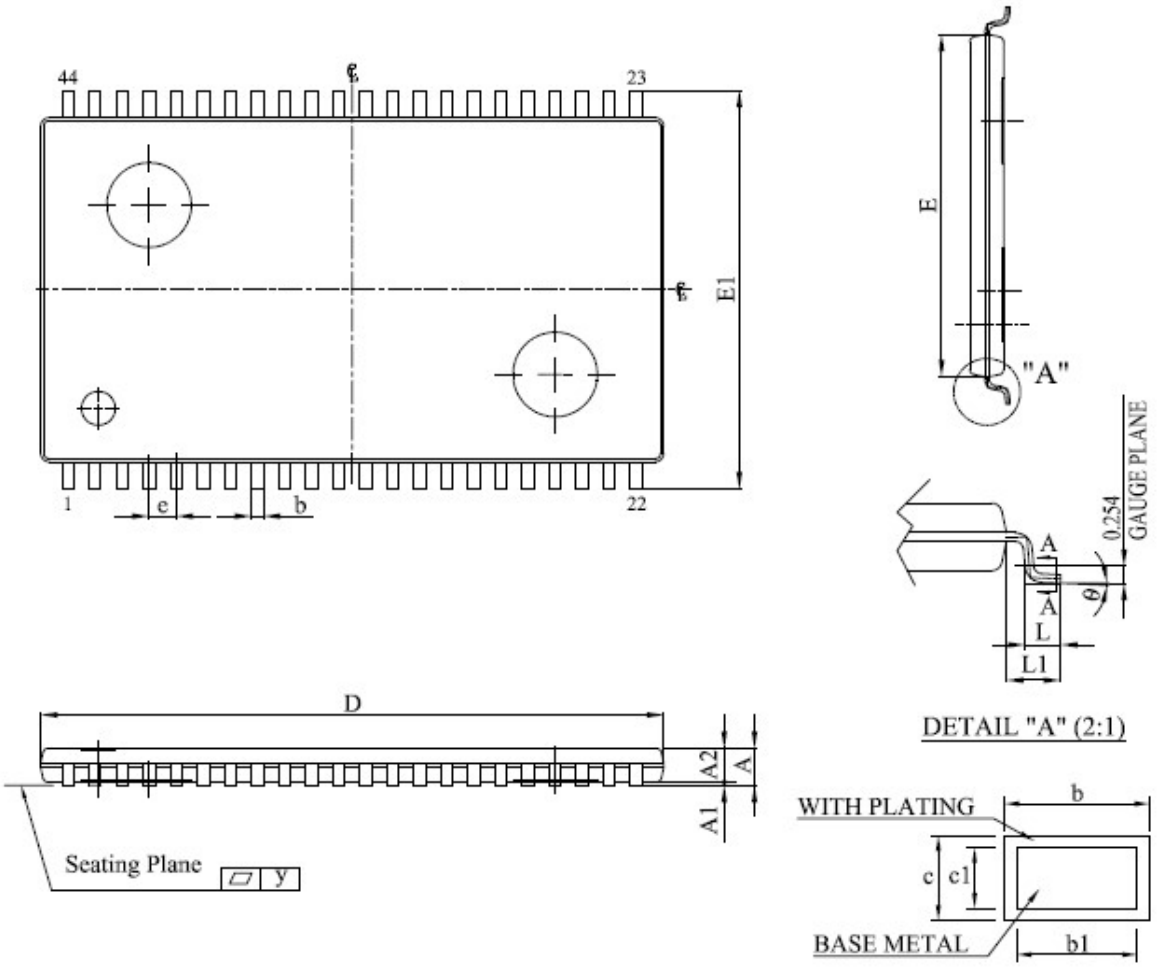
ORDER INFORMATION



Note: Package material code "P" & "R" meets RoHS

PACKAGE OUTLINE

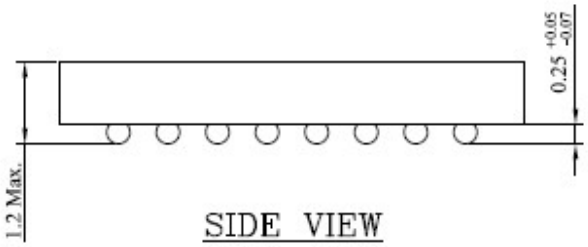
44L TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

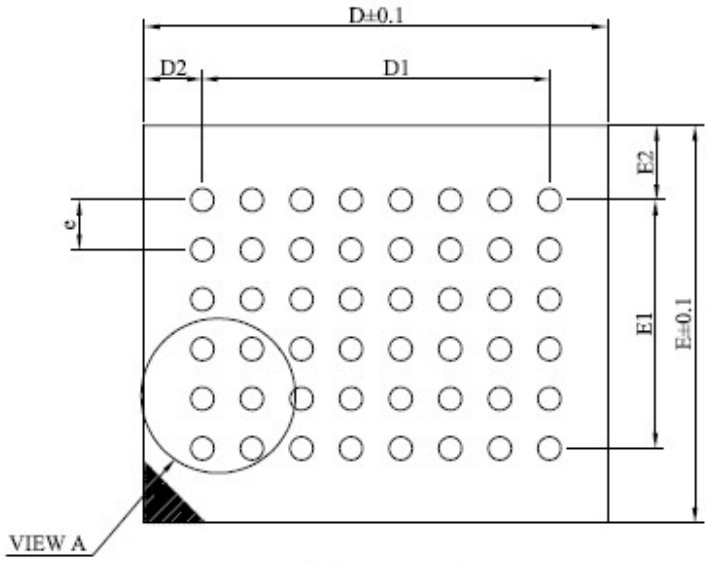
SYMBOL / UNIT		A	A1	A2	b	b1	c	c1	D	E	E1	e	L	L1	y	Θ
mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	–	0°
	Nom.	1.10	0.10	1.00	–	–	–	–	18.41	10.16	11.76	0.80	0.50	0.80	–	–
	Max.	1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	–	0°
	Nom.	0.0433	0.004	0.039	–	–	–	–	0.725	0.400	0.463	0.0315	0.0197	0.0315	–	–
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°

48 ball Mini_BGA-6X7mm

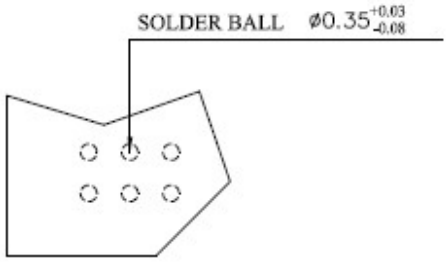


SIDE VIEW

BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
7.0	6.0	48	5.25	3.75	0.875	1.125



TOP VIEW



VIEW A

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025