



# *High Speed Super Low Power SRAM*

64K-Word By 16 Bit

**CS16LV10243**

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## Revision History

<b>Rev. No.</b>	<b>History</b>	<b>Issue Date</b>
1.0	Initial issue	Jan.17,2005
1.1	Add 48 mini_BGA & Dice	Aug. 31, 2005
1.2	Remove 48 mini_BGA	Jul. 5. 2006



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### GENERAL DESCRIPTION

The CS16LV10243 is a high performance; high speed and super low power CMOS Static Random Access Memory organized as 65,536 words by 16bits and operates from a wide range of 2.7 to 3.6V supply voltage. Advanced CMOS technology and circuit techniques provide both high speed, super low power features and maximum access time of 55/70ns in 3.0V operation. Easy memory expansion is provided by an active LOW chip enable input (/CE) and active LOW output enable (/OE).

The CS16LV10243 has an automatic power down feature, reducing the power consumption significantly when chip is deselected. The CS16LV10243 is available in JEDEC standard 44-pin TSOP 2 – 400mil package.

### FEATURES

- Wide operation voltage : 2.7 ~ 3.6V
- Ultra-low power consumption :
  - 2mA@1MHz (Max.),  $V_{CC}=3.0V$ .
  - 0.30 uA (Typ.) CMOS standby current
- High speed access time: 55/70ns.
- Automatic power down when chip is deselected.
- Three state outputs and TTL compatible.
- Data retention supply voltage as low as 1.5V.
- Easy expansion with /CE and /OE options.



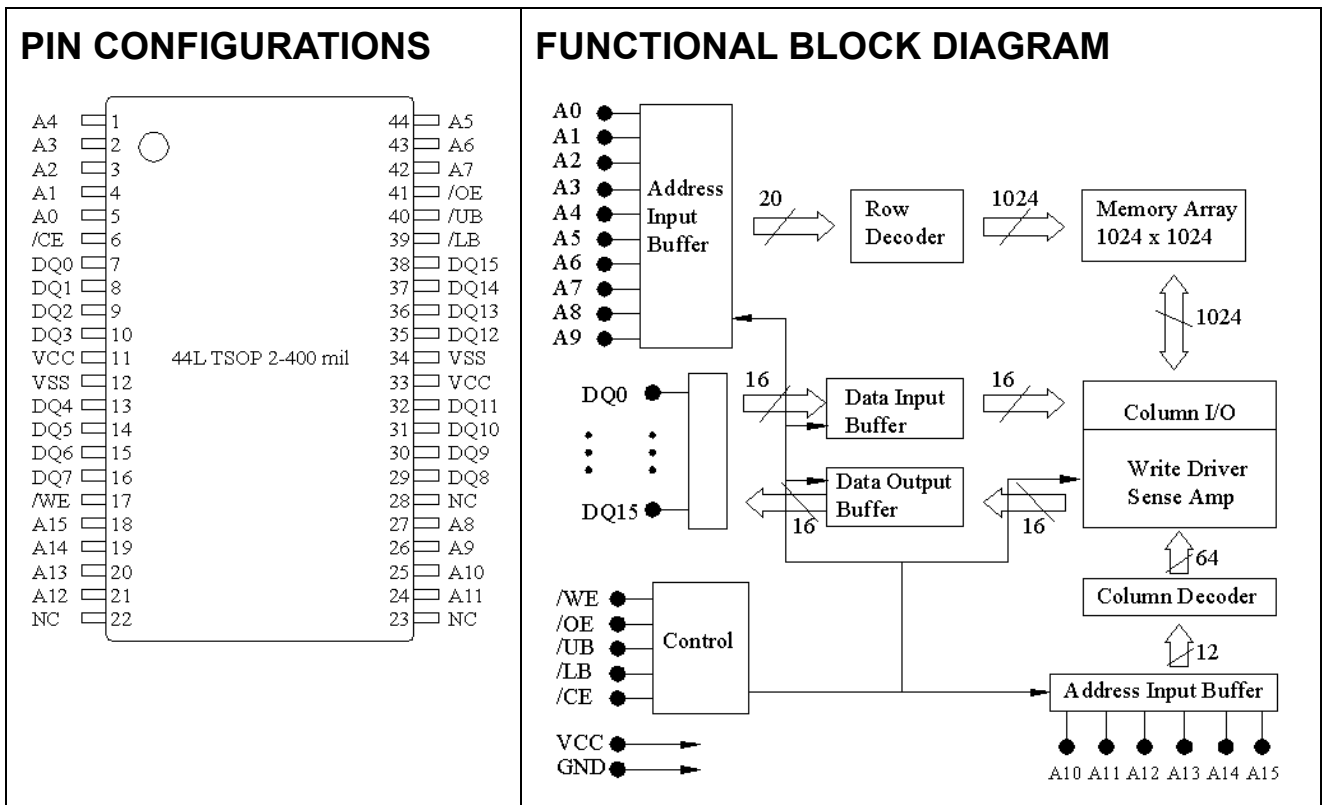
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## Product Family

Part No.	Operating Temp	V <sub>CC</sub> Range	Speed (ns)	Standby (Typ.)	Package Type
CS16LV10243	0~70°C	2.7~3.6	55/ 70	0.3 uA (V <sub>CC</sub> = 3.0V)	44L TSOP 2-400mil Dice
	-40~85°C			0.5uA (V <sub>CC</sub> = 3.0V)	





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## PIN DESCRIPTIONS

Name	Type	Function
A0 – A15	Input	Address inputs for selecting one of the 65,536 x 16 bit words in the RAM
/CE	Input	/CE is active LOW. Chip enable must be active when data read from or write to the device. If chip enable is not active, the device is deselected and in a standby power mode. The DQ pins will be in high impedance state when the device is deselected.
/WE	Input	The Write enable input is active LOW. It controls read and write operations. With the chip selected, when /WE is HIGH and /OE is LOW, output data will be present on the DQ pins, when /WE is LOW, the data present on the DQ pins will be written into the selected memory location.
/OE	Input	The output enable input is active LOW. If the output enable is active while the chip is selected and the write enable is inactive, data will be present on the DQ pins and they will be enabled. The DQ pins will be in the high impedance state when /OE is inactive.
/LB and /UB	Input	Lower byte and upper byte data input/output control pins.
DQ0~DQ15	I/O	These 16 bi-directional ports are used to read data from or write data into the RAM.
V <sub>CC</sub>	Power	Power Supply
Gnd	Power	Ground



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## TRUTH TABLE

MODE	/CE	/WE	/OE	/LB	/UB	DQ0~7	DQ8~15	V <sub>CC</sub> Current
Standby	X	X	X	H	H	High Z	High Z	I <sub>CCSB</sub> , I <sub>CCSB1</sub>
	H	X	X	X	X			
Output Disabled	L	H	H	X	X	High Z	High Z	I <sub>CC</sub>
Read	L	H	L	L	L	D <sub>OUT</sub>	D <sub>OUT</sub>	I <sub>CC</sub>
				H	L	High Z	D <sub>OUT</sub>	I <sub>CC</sub>
				L	H	D <sub>OUT</sub>	High Z	I <sub>CC</sub>
Write	L	L	X	L	L	D <sub>IN</sub>	D <sub>IN</sub>	I <sub>CC</sub>
				H	L	X	D <sub>IN</sub>	I <sub>CC</sub>
				L	H	D <sub>IN</sub>	X	I <sub>CC</sub>

## ABSOLUTE MAXIMUM RATINGS (1)

Symbol	Parameter	Rating	Unit
VTERM	Terminal Voltage with Respect to GND	-0.5 to V <sub>CC</sub> +0.5	V
TBIAS	Temperature under Bias	-40 to +125	OC
TSTG	Storage Temperature	-60 to +150	OC
PT	Power Dissipation	1.0	W
IOUT	DC Output Current	25	mA

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## OPERATING RANGE

Range	Ambient Temperature	V <sub>CC</sub>
Commercial	0~70°C	2.7V ~3.6V
Industrial	-40~85°C	2.7V ~ 3.6V

1. Overshoot : V<sub>CC</sub> +2.0V in case of pulse width ≤20ns.



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2. Undershoot : - 2.0V in case of pulse width  $\leq 20ns$ .

3. Overshoot and undershoot are sampled, not 100% tested.

## CAPACITANCE <sup>(1)</sup> (TA = 25°C, f = 1.0MHz)

Symbol	Parameter	Conditions	MAX.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> =0V	6	pF
C <sub>DQ</sub>	Input/output Capacitance	V <sub>I/O</sub> =0V	8	pF

*This parameter is guaranteed, and not 100% tested.*

## DC ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 0°C ~70°C, V<sub>CC</sub> = 3.0V)

Name	Parameter	Test Condition	MIN	TYP <sup>(1)</sup>	MAX	Unit
V <sub>IL</sub>	Guaranteed Input Low Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	-0.5		0.8	V
V <sub>IH</sub>	Guaranteed Input High Voltage <sup>(2)</sup>	V <sub>CC</sub> =3.0V	2.2		V <sub>CC</sub> +0.5	V
I <sub>IL</sub>	Input Leakage Current	V <sub>CC</sub> =MAX, V <sub>IN</sub> =0 to V <sub>CC</sub>	-1		1	uA
I <sub>OL</sub>	Output Leakage Current	V <sub>CC</sub> =MAX, /CE=V <sub>IH</sub> , or /OE=V <sub>IH</sub> , or /WE=V <sub>IL</sub> V <sub>I/O</sub> =0V to V <sub>CC</sub>	-1		1	uA
V <sub>OL</sub>	Output Low Voltage	V <sub>CC</sub> =MAX, I <sub>OL</sub> =2.1mA			0.4	V
V <sub>OH</sub>	Output High Voltage	V <sub>CC</sub> =MIN, I <sub>OH</sub> =-1.0mA	2.4			V
I <sub>CC</sub>	Operating Power Supply Current	/CE=V <sub>IL</sub> , I <sub>DQ</sub> =0mA, F=F <sub>MAX</sub> =1/ t <sub>RC</sub>			25	mA
I <sub>CCSB</sub>	TTL Standby Supply	/CE=V <sub>IH</sub> , I <sub>DQ</sub> =0mA,			0.5	mA
I <sub>CCSB1</sub>	CMOS Standby Current	/CE $\geq$ V <sub>CC</sub> -0.2V, V <sub>IN</sub> $\geq$ V <sub>CC</sub> -0.2V or V <sub>IN</sub> $\leq$ 0.2V,		0.3	4	uA



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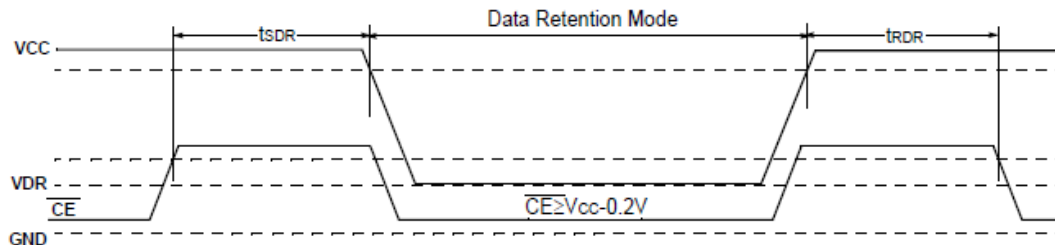
1. Typical characteristics are at  $T_A = 25^\circ\text{C}$ .
2. These are absolute values with respect to device ground and all overshoots due to system or tester noise are included.
3.  $F_{\text{max}} = 1/t_{\text{RC}}$ .

## DATA RETENTION CHARACTERISTICS ( $T_A = 0^\circ\text{C} \sim 70^\circ\text{C}$ )

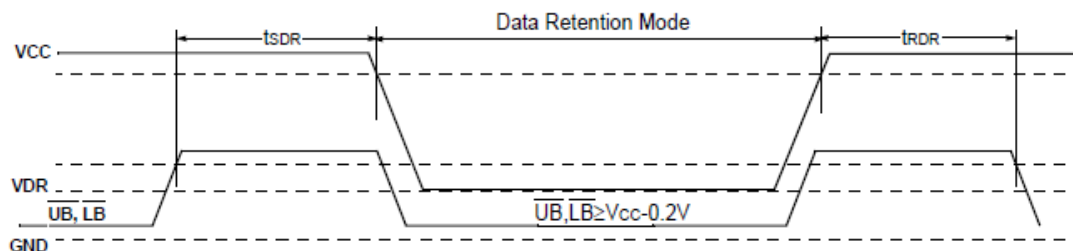
Name	Parameter	Test Condition	MIN	TYP <sup>(1)</sup>	MAX	Unit
$V_{\text{DR}}$	$V_{\text{CC}}$ for Data Retention	$V_{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$ , $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$	1.5			V
$I_{\text{CCDR}}$	Data Retention Current	$V_{\text{CE}} \geq V_{\text{CC}} - 0.2\text{V}$ , $V_{\text{CC}} = 1.5\text{V}$ $V_{\text{IN}} \geq V_{\text{CC}} - 0.2\text{V}$ or $V_{\text{IN}} \leq 0.2\text{V}$		0.2	2	$\mu\text{A}$
$T_{\text{CDR}}$	Chip Deselect to Data Retention Time	Refer to Retention Waveform	0			ns
$t_{\text{R}}$	Operation Recovery Time		$t_{\text{RC}}(2)$			ns

1.  $T_A = 25^\circ\text{C}$ , 2.  $t_{\text{RC}}$  = Read Cycle Time

### LOW $V_{\text{CC}}$ DATA RETENTION WAVEFORM (1) (/CE Controlled)



### LOW $V_{\text{CC}}$ DATA RETENTION WAVEFORM (2) (/UB, /LB Controlled)





### AC TEST CONDITIONS

Input Pulse Levels	V <sub>cc</sub> /0V
Input Rise and Fall Times	5ns
Input and Output Timing Reference Level	0.5V <sub>cc</sub>
Output Load	See FIGURE 1A and 1B

### KEY TO SWITCHING WAVEFORMS

WAVEFORMS	INPUTS	OUTPUTS
	MUST BE STEADY	MUST BE STEADY
	MAY CHANGE FROM H TO L	WILL BE CHANGE FROM H TO L
	MAY CHANGE FROM L TO H	WILL BE CHANGE FROM L TO H
	DON'T CARE ANY CHANGE PERMITTED	CHANGE STATE UNKNOWN
	DOES NOT APPLY	CENTER LINE IS HIGH IMPEDANCE OFF STATE

### AC TEST LOADS AND WAVEFORMS

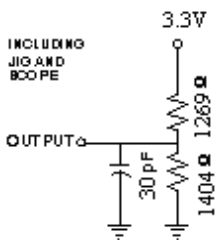


FIGURE 1A

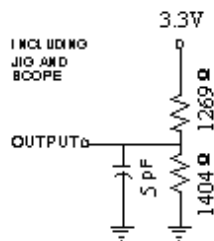
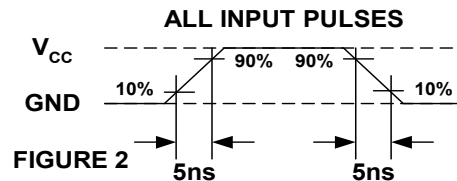
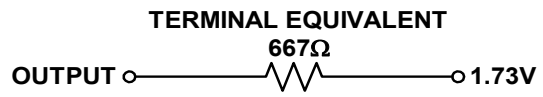


FIGURE 1B





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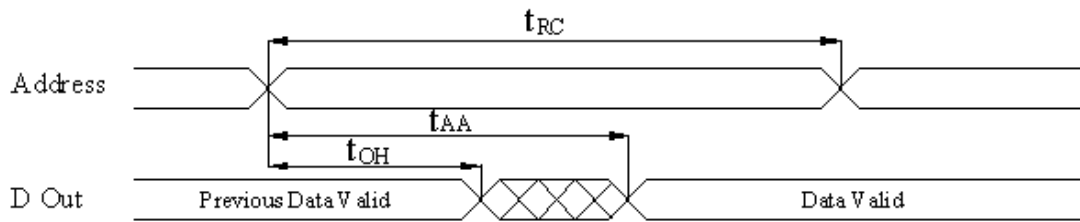
## AC ELECTRICAL CHARACTERISTICS ( $T_A = 0^\circ\text{C} \sim 70^\circ\text{C}; V_{CC} = 3.0\text{V}$ )

### READ CYCLE

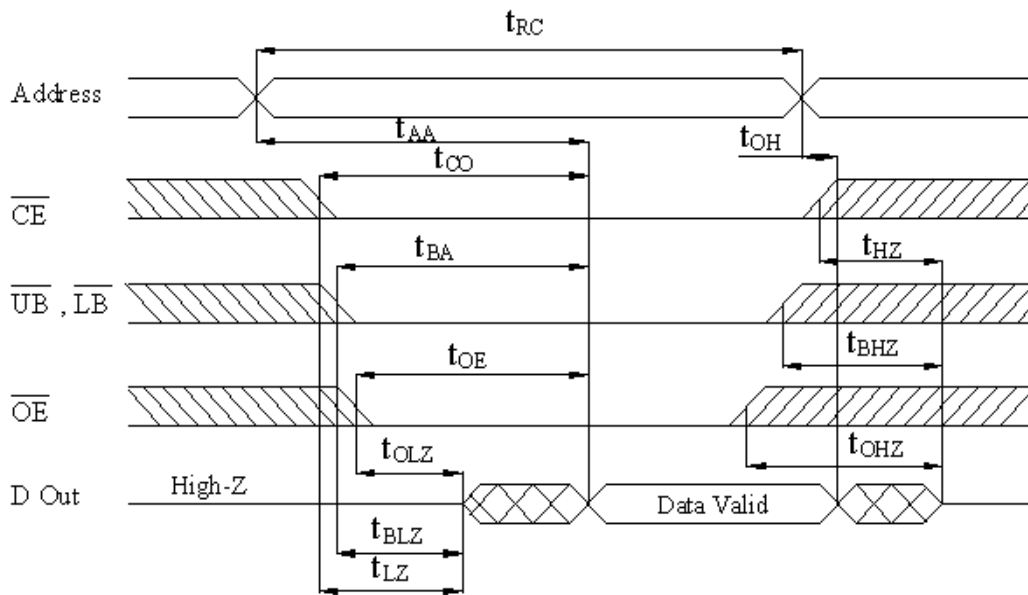
JEDEC Parameter Name	Parameter Name	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
$t_{AVAX}$	$t_{RC}$	Read Cycle Time	55		70		ns
$t_{AVQV}$	$t_{AA}$	Address Access Time		55		70	ns
$t_{ELQV}$	$t_{CO}$	Chip Select Access Time (/CE)		55		70	ns
$t_{BA}$	$t_{BA}$	Data Byte Control Access Time (/LB, /UB)		55		70	ns
$t_{GLQV}$	$t_{OE}$	Output Enable to Output Valid		25		35	ns
$t_{ELQX}$	$t_{LZ}$	ChiChip Select to Output Low Z (/CE)	10		10		ns
$t_{BE}$	$t_{BLZ}$	Data Byte Control to Output Low Z (/LB, /UB)	5		5		ns
$t_{GLQX}$	$t_{OLZ}$	Output Enable to Output in Low Z	5		5		ns
$t_{EHQZ}$	$t_{HZ}$	Chip Deselect to Output in High Z (/CE)	0	20	0	25	ns
$t_{BDO}$	$t_{BHZ}$	Data Byte Control to Output High Z (/LB, /UB)	0	20	0	25	ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	20	0	25	ns
$t_{AXOX}$	$t_{OH}$	Out Disable to Address Change	10		10		ns

### SWITCHING WAVEFORMS (READ CYCLE)

#### READ CYCLE1



#### READ CYCLE2



#### NOTES:

1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the outputs achieve the open circuit conditions and are not referenced to output voltage levels.
2. At any given temperature and voltage condition,  $t_{HZ}(\text{Max.})$  is less than  $t_{LZ}(\text{Min.})$  both for a given device and from device to device interconnection.



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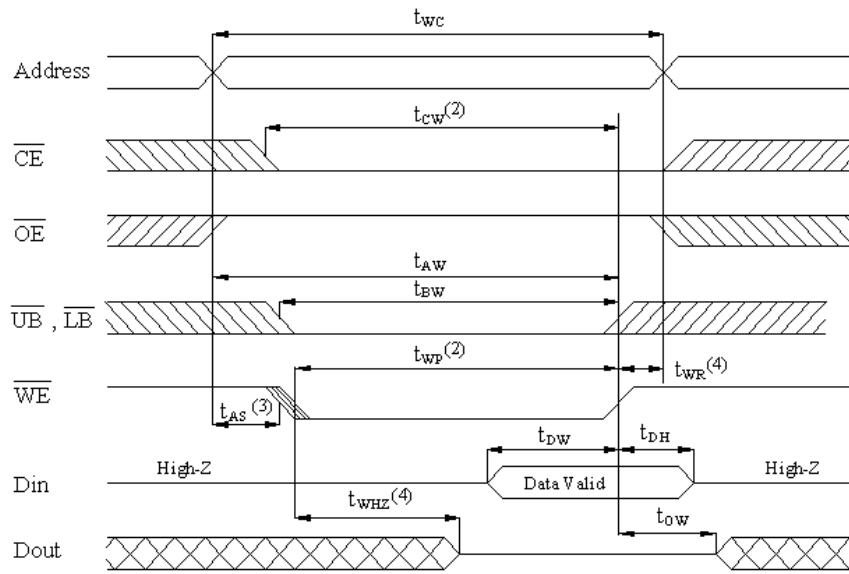
## AC ELECTRICAL CHARACTERISTICS ( $T_A = 0^\circ\text{C} \sim 70^\circ\text{C}; V_{CC} = 3.0\text{V}$ )

### WRITE CYCLE

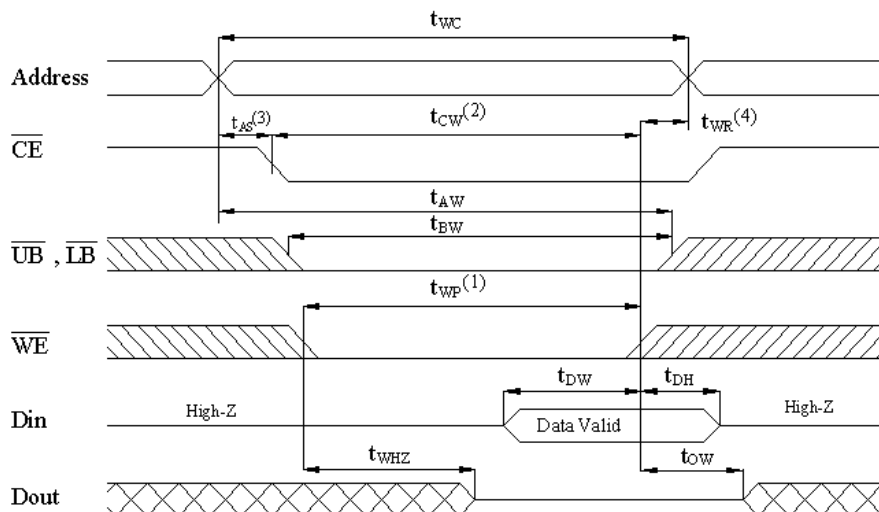
JEDEC Name	Symbol	Description	-55		-70		Unit
			MIN	MAX	MIN	MAX	
$t_{AVAX}$	$t_{WC}$	Write Cycle Time	55		70		ns
$t_{E1LWH}$	$t_{CW}$	Chip Select to End of Write	45		60		ns
$t_{AVWL}$	$t_{AS}$	Address Setup Time	0		0		ns
$t_{AVWH}$	$t_{AW}$	Address Valid to End of Write	45		60		ns
$t_{BW}$	$t_{BW}$	/UB, /LB valid to end of write	45		60		ns
$t_{WLWH}$	$t_{WP}$	Write Pulse Width	40		50		ns
$t_{WHAX}$	$t_{WR}$	Write Recovery Time	0		0		ns
$t_{WLQZ}$	$t_{WHZ}$	Write to Output in High Z		25		30	ns
$t_{DVWH}$	$t_{DW}$	Data to Write Time Overlap	25		30		ns
$t_{WHDX}$	$t_{DH}$	Data Hold for Write End	0		0		ns
$t_{GHQZ}$	$t_{OHZ}$	Output Disable to Output in High Z	0	30	0	30	ns
$t_{WHOX}$	$t_{OW}$	End of Write to Output Active	5		5		ns

### SWITCHING WAVEFORMS (WRITE CYCLE)

#### WRITE CYCLE1 (/WE CONTROLLED)



#### WRITE CYCLE2 (/CE CONTROLLED)



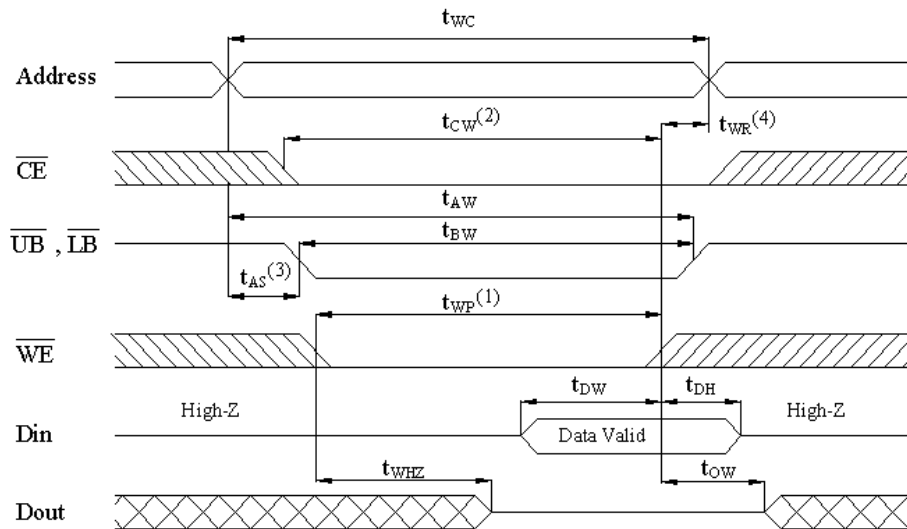


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## WRITE CYCLE3 (/UB, /LB CONTROLLED)

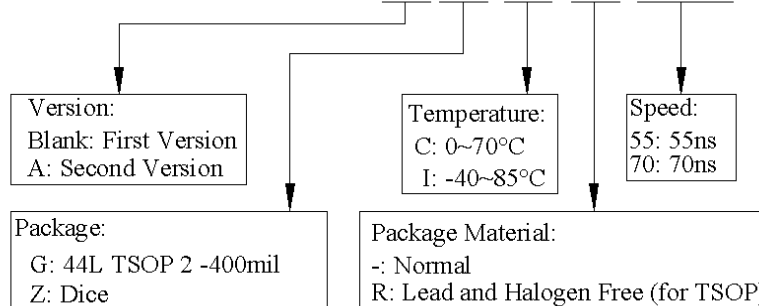


**NOTES:**

1. A write occurs during the overlap ( $t_{WP}$ ) of low /CE and low /WE. A write begins when /CE goes low and /WE goes low with asserting /UB and /LB for double byte operation. A write ends at the earliest transition when /CE goes high and /WE goes high. The  $t_{WP}$  is measured from the beginning of the write to the end of write.
2.  $t_{CW}$  is measured from the /CE going low to end of write.
3.  $t_{AS}$  is measured from the address valid to the beginning of write.
4.  $t_{WR}$  is measured from the end of write to the address change.  $t_{WR}$  applied in case a write ends as /CE or /WE going high.

## ORDER INFORMATION

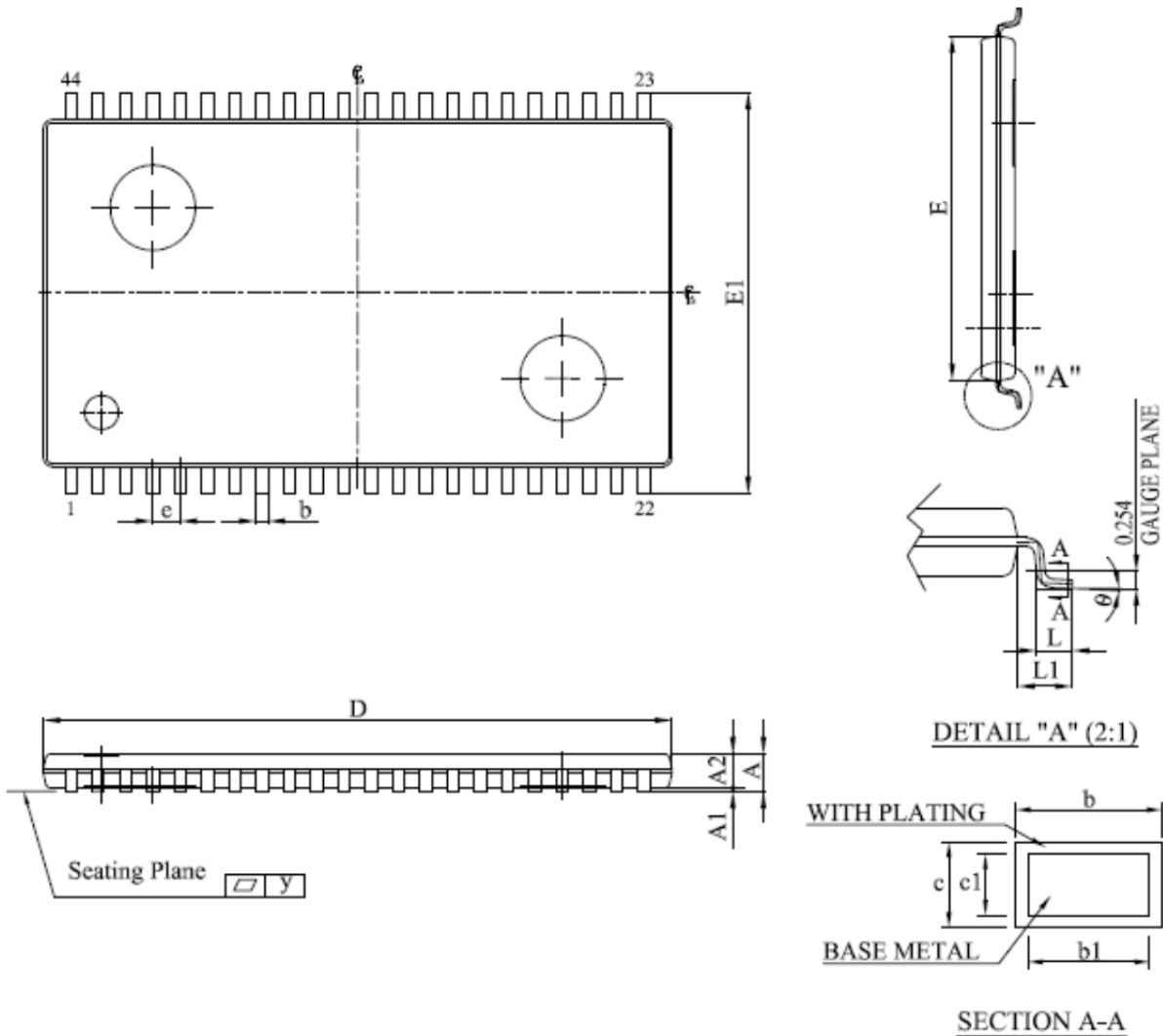
CS16LV10243 X X X X XX



Note: Package material code "R" meets ROHS

### PACKAGE OUTLINE

#### 44L TSOP2-400mil



Note: Plating thickness spec : 0.3 mil ~ 0.8 mil.

SYMBOL UNIT	A	A1	A2	b	b1	c	cl	D	E	E1	e	L	L1	y	θ	
	mm	Min.	1.00	0.05	0.95	0.30	0.30	0.12	0.12	18.31	10.06	11.56	0.70	0.40	0.70	-
Nom.		1.10	0.10	1.00	-	-	-	-	18.41	10.16	11.76	0.80	0.50	0.80	-	-
Max.		1.20	0.15	1.05	0.45	0.40	0.21	0.16	18.51	10.26	11.96	0.90	0.60	0.90	0.1	8°
inch	Min.	0.0393	0.002	0.037	0.012	0.012	0.005	0.005	0.721	0.396	0.455	0.0275	0.0157	0.0275	-	0°
	Nom.	0.0433	0.004	0.039	-	-	-	-	0.725	0.400	0.463	0.0315	0.0197	0.0315	-	-
	Max.	0.0473	0.006	0.041	0.018	0.016	0.008	0.006	0.729	0.404	0.471	0.0355	0.0237	0.0355	0.004	8°