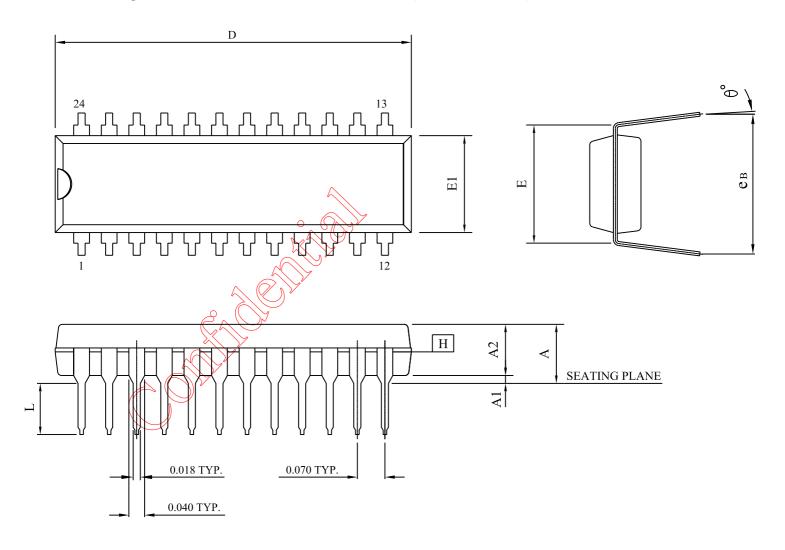


晶發半導體股份有限公司

Chiplus Semiconductor Corp.

Title: Package outline for 24Shrink PDIP-300mil (Pitch 0.07 inch)



NOTES:

- 1.JEDEC OUTLINE: MS-019 AF
- 2."D","E1" DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH.
- 3.eB IS MEASURED AT THE LEAD TIPS WITH THE LEADS UNCONSTRAINED.
- 4.POINTED OR ROUNDED LEAD TIPS ARE PREFERRED TO EASE INSERTION.
- $5. DISTANCE\ BETWEEN\ LEADS\ INCLUDING\ DAM\ BAR\ PROTRUSIONS\ TO\ BE\ .005\ INCH\ MININUM.$
- 6.DATUM PLANE \blacksquare COINCIDENT WITH THE BOTTOM OF LEAD, WHERE LEAD EXITS BODY.
- 7.PLATING THICKNESS: $0.3 \sim 0.8$ MIL.

SY	MBOL	A	A1	A2	D	E	E1	L	СВ	θ°
inch	Min.	-	0.015	0.125	0.880	0.300 BSC.	0.245	0.115	0.335	0°
	Nom.	-		0.130	0.900		0.250	0.130	0.355	7°
	Max.	0.210	_	0.135	0.920	DSC.	0.255	0.150	0.375	10°

DWG. NO.	ORIGINATOR	ISSUE DATE	REV.
PC600-0019	Yuki Yeh	24-Apr'08	0